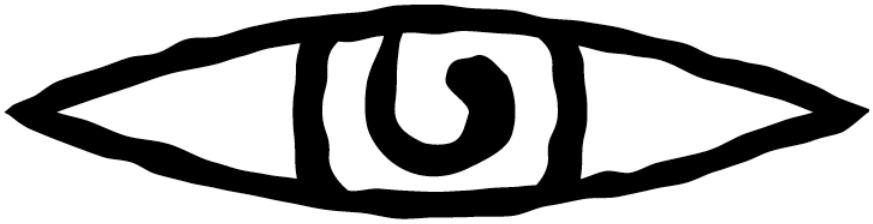

ASTEC

Advanced Software Technology

Report for Phase 4,
the final phase.
Year 9-10
2004-2005

UPPSALA
UNIVERSITET

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2007-09-26

ASTEC
Advanced Software Technology

ASTEC Report for phase 4, 2004-2005

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1. Summary

Important project results are the automatic software analyser "Dialyzer" that has been designed, implemented and already is used by industry. Several case studies of industrial software have been carried out using the WCET tool. This has increased the knowledge about the WCET method at the industrial partners. The economy follows on the whole the budget, diminished contributions by some partners has been compensated by increased contributions by other partners.

1. Sammanfattning

Viktiga projektresultat som framkommit under året är att den automatiska programanalysatorn "Dialyzer" har designat, implementerats och även börjat användas av industrin. Ett flertal studier av industriell programvara har utförts med WCET verktyget vilket ökat medvetenheten om dess användbarhet i industrin. Ekonomin följer i stort sett planeringen minskade insatser av några parter har kompenserats av ökade insatser från andra parter.

2. Research activities and co-operation

At the negotiation meeting in January 2004 at VINNOVA the participants agreed on starting the final phase of ASTEC. At the preceding process of discussions a set of research projects was formed (Table 1). These projects were composed to meet the needs from industry for pre and non-competitive research as well as exploring new areas and to be able to maintain and further develop software products with a long history of development and improvements. This software often forms the core in major products from the partners. The projects also meet the Academic demands for training PhD and M. Sc students as well as to provide top of the line research challenges. The projects were also selected to fit into the technical and application areas of ASTEC (Table 2). Some projects are mature entering or continuing the "commercialization phase", such as HiPE and WCET, others were initiated by new demands from industry, like PLEX and Remodel, that are exploiting the ability to solve complex problems that is found in academia.

Changes after the initial negotiation
- Eurocontrol had to withdraw from ASTEC since it was not possible for them to join a Competence centre. The project is carried out outside ASTEC in Uppsala.
- Validation AB were split between WM-Data Validation AB and Telia AB.
- IAR has been bought by NOCOM AB during 2005.
- Volcano Communication Technologies has been bought by Mentor Graphics (Scandinavia) AB during 2005.
- T-Mobile Inc. could not join ASTEC; personal contacts are continued outside ASTEC.

During 2004 ASTEC carried out research according to the activity plan in the two application and three technical areas (Table 1). The ten projects finally selected cover all areas, a few projects have activities in two or three areas (Table 2). The volume for each project is given in table 3. All projects have close industrial co-operation with one or several partners. ASTEC calculates each year a number of business ratios to follow-up the development as a competence centre (Appendix 1). ASTEC recovered from the stagnation in growth during 2001-2003 and has 2004 achieved the highest activity during its existence. The publication rate dropped a bit during 2004, a phenomenon also seen at the start of previous phases.

Table 1. Project acronyms, names and goals.

Acronym	Name	Goal
HiPE	High Performance Erlang	To develop techniques for efficient compilation of concurrent functional programming languages.
SAAPP	Simulator-Aided Analysis of Parallel Processes	To monitor and analyse the execution of parallel programs at runtime, in a predictable and reproducible way, in order to find race conditions and other dependencies between processes.
Fault Tree Analysis		To develop tools to perform Fault Tree Analysis on time-dependent safety-critical systems.
AuToWay	Automatic Testing of a WAP Gateway	The testing cluster at ASTEC. The 3 projects focuses on techniques for automated testing of computer systems. Central problems are: - Symbolic techniques for generation of test suites from abstract models of system under test. - Generation of test oracles from requirements of systems under test.
DeTrack	Tracking Dependencies in Software Modules	
STEP	Specification Testing environment for Erlang Protocol software	
WPO	Whole Programme Optimization	To explore optimization techniques that become feasible when the entire program is available to the compiler. We focus on optimizations that reduce memory use.
REMODEL		To provide methods and tools for introducing timing analysis in existing industrial software systems.
PLEX		Methods to parallelize PLEX programs.
WCET	Worst Case Execution Time Analysis	A WCET prototype tool, containing all parts (flow analysis, pipeline analysis, cache analysis, WCET calculation).

Table 2. The technical and application areas covered by ASTEC.

Technical area / Application area	Validation and verification	Programming Language Implementation and Compilation	Real-Time Embedded, and Distributed Systems
Software for Data- and Telecommunication Systems	AuToWay DeTrack STEP Testing Fault Tree Analysis	HiPE PLEX	HiPE Remodel
Software for Embedded Applications	SAAPP Remodel Fault Tree Analysis	WCET WPO	Remodel WCET

Table 3. ASTEC Research projects during phase 4.
Project leaders, volume and the partner's contributions are given.

Project	**Leader**	**Total**[1] (MSEK)	**Industral Partners**[2]	**Vinnova** (MSEK)	**Industry** (MSEK)	**Academy** (MSEK)
HiPE	Kostis Sagonas	9,6	7, 12	3,9	2,8	2,9
SAAPP	Björn Victor	2,4	15	0,9	0,8	0,8
Fault Tree Analysis	Parosh Abdulla	4,8	11	0,7	3,5	0,6
AuToWay	Paul Pettersson	3,1	8	1,2	0,9	1,0
DeTrack	Bengt Jonsson	1,7	14	0,5	0,2	0,9
STEP	Bengt Jonsson	2,7	10	0,7	1,0	1,0
WPO	Sven-Olof Nyström	1,3	9	0,3	0,7	0,3
REMODEL	Christer Norström	6,3	1	2,1	2,0	2,1
PLEX	Björn Lisper	2,4	6	0,5	1,3	0,7
WCET	Björn Lisper	6,5	2, 3, 4, 5, 13, 16	1,9	3,1	1,3
Admin		2,3		1,4		0,9
SUM		**43,0**		**14,2**	**16,3**	**12,6**

1) Total = all contributions
2) For industrial partners list see table 4.

Table 4, **ASTEC industrial partners active during phase 4.**

1 ABB Automation Technologies AB
2 AbsInt Angewandte Informatik GmbH
3 Arcticus Systems AB
4 Cross Country Systems AB
5 ENEA Embedded Technology AB
6 Ericsson AB (the departments APZ, UKI/O and KI/EAB)
7 I.A.R. Systems AB
8 Mobile Arts AB
9 Prover Technology AB
10 TIDORUM AB
11 WM data Validation AB
12 Virtutech AB
13 Volvo Teknisk Utveckling AB

3. The international standing of ASTEC

ASTEC researchers are firmly established in the international research community. Senior researchers are members of program committees in key conferences of the areas of the strategic research plan.

A sign of recognition is that the TIMES tool received the best tool award at the ETAPS conferences in April 2002, and that ASTEC has been invited to present its activities in a special issue of the Springer Verlag journal STTT (Software Tools for Technology Transfer).

ASTEC has a strong network of international contacts. As examples, the UPPAAL and TIMES projects have been collaborating very closely with Aalborg University in Denmark since 1995. ASTEC groups have had a long been an active collaboration with Seoul National University (SNU) (Andreas Ermedahl (then an ASTEC Ph.D. student) has been on a 6 month visit at SNU), and with C-Lab in Paderborn, Germany (including frequent visits by Friedhelm Stappert)

In addition to visits within the collaboration just mentioned, ASTEC attracts both long- and short-term visitors. Prof. Werner Damm, Univ. of Oldenburg, has spent a semester as visiting professor in autumn 2001, Prof. Yih-Kuen Tsay, National Univ. of Taiwan, June- Sept. 2005.ASTEC groups have hosted several post-doc researchers from other countries. Yves Boussemart, MIT and Raimund Kirner, TU Wien has visited Mälardalen University.

Through its partners, ASTEC has participated in several European Community research projects.

* The ARTIST2 (Advanced Real Time Systems) Network of Excellence, in which Mälardalen University and Uppsala University participate as area coordinator, collects around 30 leading research groups in Europe with the objectives to coordinate European Research and Development effort in the area of Advanced Real-time Systems, e.g., by identifying innovative and relevant research directions. Mälardalen University is Core partner i ARTIST2-clustret on Compilers and Timing Analysis

* The GAMES Research and Training network GAMES, comprising 7 European and 1 U.S. University is concerned with developing techniques for the synthesis and validation of computing systems that are based on games and automata.

ASTEC partners also participated in several national projects, e.g.,

* SAVE (Component Based Design of Safety Critical Vehicular Systems), which is a national project supported by SSF (Swedish strategic research). The goal of the project is to establish an engineering discipline for systematic development of component-based software for safety critical embedded vehicular systems. Uppsala's effort within SAVE will be focused on component models and verification of quantatative properties of components.
* The PROGRESS centre has been selected as a strategic research centre by SSF for the period 2006-2011.

ASTEC has co-organized and co-sponsored several international workshops and conferences, including PLI'03 (Principles, Logics and Implementations of High-Level Programming Languages) which comprises of ICFP (ACM SIGPLAN International Conference on Functional Programming), PPDP (ACM SIGPLAN Conference on Principles and Practice of Declarative Programming), and a total of five co-located workshops. The 16th Nordic Workshop on Programming Theory (NWPT'04) was held at Uppsala University, October 6-8, 2004. The 3rd FORMATS (International Conference on Formal Modelling and Analysis of Timed Systems) was held in Uppsala, Sweden, September 26 - 28, 2005 in conjunction with ARTIST2 summer school, September 29 - October 2, 2005, on Component Modelling, Testing and Verification, and Static analysis of embedded systems. Furthermore has the meetings ETFA2004, ETFA2005 and WFCS2004 been co-organized by ASTEC staff.

A collection of scientific papers, which represent ASTEC work, were invited and published 2003 in the Springer Verlag journal STTT (International Journal on Software Tools for Technology), together with a cover paper which presents the ASTEC framework, with the goal of presenting ASTEC to a wider scientific community.

ASTEC conducts technical seminars, and seminars directed to an industrial audience. For example, Jakob Engblom gave a lecture on efficient C programming for embedded systems, on behalf of IAR Systems, at the Embedded Systems Conferences in San Francisco in 2001 and 2002. The lecture topic was how to write code that is efficiently compiled by a modern C compiler. Open half-day seminars are organized to present results of selected ASTEC project clusters.

4. Evaluations

At the "ASTEC Scientific Advisory Day in September 2004" the Scientific Advisory Board comprising of Neil Jones (University of Copenhagen), Bernhard Steffen (University of Dortmund) and Neeraj Suri (TU Darmstadt) gave comments on projects for the remaining period (Appendix 2). The concluding remark by the advisors really boosts our self-esteem. "Overall, we emphatically feel that ASTEC has developed over the years to be considered a success story for a competence centre. Its development of competence in SW within Sweden is undisputed, and has made its mark as a leading centre worldwide! Given its academic and applied impact, we strongly support any efforts that would help sustain (& increase) the essence of this competence for the years ahead."

Not just the size, but also the quality of the IT Department in Uppsala is unique for Sweden. According to the bibliometric study based on the ISI Web of Knowledge commissioned by the university president, Uppsala IT research is well ahead of other sites in Sweden also in terms of its quality as measured as citations per paper. In that study Uppsala's IT Department ranked the third best in Europe. The very group behind this proposal shows particular strength in such studies. In an investigation of the local Linnaeus nominees carried out by the University (Oct.21, 2005) the DMACS research constellation (i.e. partly ASTEC researchers) yields an index of "citations per publication" of 2.2. Such a high score is typical of world-class groups.

Students at the "Department of History of Science and Ideas" studied ASTEC from the centre point of view. The report1 show a positive view of ASTEC and that we have come to similar conclusions as VINNOVA in their studies on how a centre should function.

5. Research results and their effect on ASTEC partners

WPO (Whole Programme Optimization) and **DeTrack** has contributed to the industrial partners potential for future development of existing products. However due to circumstances outside the control of the persons directly involved in the projects, have the industrial partners switched priorities. Both industries have changed owners since the start of phase 4. This has resulted in activities to finalize the projects.

At the **DeTrack** project, a technique for detecting dependencies was developed and implemented. The technique has been used to detect dependencies in a system module under test at Validation AB. The results have been validated with system experts at Validation AB.

The **Remodel** project includes research groups at ABB, Uppsala University and Mälardalens högskola in a joint effort on modelling the ABB Robotics system. The ASTEC-supported past development of the UPPAAL and TIMES tools has been used to model and simulate systems with timing and stochastic behaviours. The project is highly promising to create a model of great use for ABB Robotics. A set of three tools has already been developed. One project member, Anders Wall, has been hired by ABB as a researcher from November 2004.

The software testing project **AutoWay** (Automatic Testing of a WAP Gateway) is developing a method for model based testing of Real-Time systems (the WAP Gateway) using the same tools (UPPAAL and Times) as the Remodel project. A formal model of the WAP Gateway has been produced and implementation of a test case generator is ready. A PhD student has visited Ericsson for 2 weeks to study the WAP Gateway. Anders Hessel made his Licentiate thesis in February 2006 and followed up with a PhD in May 2007.

The testing project **STEP** (Specification Testing environment for Erlang Protocol software) A tool for test case generation has been developed. This tool has been used to generate test suites from a specification of a product at Mobile Arts. The tool will be released to the community of Erlang developers. Co-operation is planned with the AutoWay project on test case generation for WAP Gateway in collaboration with Ericsson AB.

The **Fault Tree Analysis** project is developed in collaboration with Prover Technology

[1] ASTEC– forskning i kompetenscentrum. Caroline Isaksson, Karin Lindström, Mathias Possnert, Pablo Ortiz Elgueta, Ulf Troeng, Zandra Cedén, Handledare: Jenny Beckman, Uppsala Universitet 2006-03-10, Institutionen för Idé och lärdomshistoria, Teknik- och vetenskapshistoria, 5 p STS 2.

through its involvement in the EC project ISAAC, Prover Technology has contacts with aircraft manufacturers (Airbus, Saab, Dassault, Alenia). Airbus uses Scade to model systems from an abstract point of view and to design concrete components. Since Scade's code generator is a certified tool, it can be used to automatically generate software which can be executed on systems embedded into civil aircrafts. This automated code generation helps to avoid bugs introduced by humans while programming, but it is still necessary to validate the specification. Esterel Technologies addressed this issue with their Scade Design Verifier, which is built on top of Prover's model checker. Today, the version of Scade available for sale includes Prover's model checker. Fault Tree Analysis, which we developed within ASTEC, may be included in future versions of the Design Verifier. Airbus is currently evaluating the FTA tool on actual subsystems of their aircrafts.

Due to its set-up the project has a lot of international cooperation besides the industries mentioned above. We cooperate with ITC-IRST (www.itc.it/irst), in the area of hybrid model checking. To allow continuous dense time and thereby a more realistic modelling.

ONERA/Cert (www.cert.fr), is responsible for the Common Cause Analysis with ISAAC. In Fault Tree Analysis, a common assumption is that failure of components are independent. This is not a very realistic assumption, since a single event e.g. a lightning may cause several failures to happen simultaneously. A requirement for reliable systems is that no combination of n failures may cause the system to become unsafe. Parameter n is chosen according to the required level of reliability of the system. In order to take into account common causes of component failures, the above statement should be modified: “ No combination of n independent failures may cause the system to be unsafe”. We are currently cooperating with ONERA to modify the existing implementation to support common causes.

OFFIS (www.offis.de) uses Statemate to model systems, and Prover's model checker for verification. OFFIS is responsible for the Human Error Analysis section of ISAAC, which assesses effects of human errors on the safety of the aircraft. A model of the pilot is made from documents describing usual procedures (refuel in air, landing...). Then failures are injected into the model, thus modelling the possibility of human errors i.e. deviations from the documented procedures. This methodology is very similar to Fault Tree Analysis, where hardware failures are replaced with human errors. OFFIS is investigating the possibility to use Prover's model checker to perform the analysis, similarly to the method we developed to perform Fault Tree Analysis using a model checker. Saab provides procedure descriptions.

Johann Deneux made his dissertation 2006-06-02 on the thesis "Verification of Parameterized and Timed Systems: Undecidability Results and Efficient Methods".

The **HiPE** (High Performance Erlang) project research results in optimizations for the worldwide Erlang community and specifically for Ericsson. Here is this phase results

Correctness analysis of Erlang programs
In safety-critical and high-reliability systems, software development and maintenance are costly endeavours. The cost can be reduced if software errors can be identified through automatic tools such as program analyzers and compile-time software checkers. To this effect, we have recently designed and implemented a software tool, called Dialyzer. Dialyzer uses lightweight static analysis to detect discrepancies (i.e., software defects such as exception-raising code or hidden failures) in large commercial telecom applications written in Erlang. Dialyzer, starting from virtual machine bytecode, discovers, tracks, and propagates type information which is often implicit in Erlang programs, and reports warnings when a variety of type errors and other software discrepancies are identified. Since the analysis currently starts from bytecode, it is completely automatic and does not rely on any user annotations.

Moreover, it is effective in identifying software defects even in cases where source code is not available, and more specifically in legacy software which is often employed in high-reliability systems in operation, such as telecom switches. With the help of our industrial partners, we have applied our tool to a handful of real-world applications, each consisting of several hundred thousand lines of code, and described our experiences and the effectiveness of our techniques in a paper presented at APLAS'04. The Dialyzer tool has been extremely successful. It has been adopted by many Erlang projects and will soon be incorporated in the Ericsson's development environment of GPRS, AXD301, and T-Mobile's.

A HiPE compiler for AMD64 machines
The first 64-bit back-end of the HiPE compiler, has been developed and reached the robustness and maturity of the SPARC and x86 back-ends. Performance results show that the resulting system, HiPE/AMD64, is significantly faster than the default virtual machine-based implementation of Erlang, and achives speedups comparable to and sometimes better than those of the more mature HiPE/SPARC and HiPE/x86 compilers. The HiPE/AMD64 compiler was included in the Erlang/OTP release 10 (R10) by Ericsson in October 2004.

A better exception mechanism for Erlang
Working in collaboration with the implementors of Erlang/OTP, we designed and developed a better exception mechanism based on a try/catch construct, similar to that used in Java. Ericsson has integrated a complete implementation of the mechanism in Erlang/OTP in release R10B.

Design of compilation techniques for adaptive pattern matching over binary data
Pattern matching is an important operation in functional programs. We have presented an approach to extend pattern matching to terms without (much of a) structure such as binaries which is the kind of data format that network applications typically manipulate. The effectiveness of our techniques was evaluated using implementations of network protocols taken from telecom applications. The overall performance of the proposed scheme was shown to be competitive with versions of the same application written in a low-level language such as C.

The **SAAPP** (Simulator-Aided Analysis of Parallel Processes) project has created contacts between SICS (the Time Bending project), the EU project RUNES, Virtutech AB and ENEA Embedded Technology AB in the efforts to detect and debug race conditions. A tool for the detection has been developed.

The **WCET** (Worst Case Execution Time Analysis) project has during 2004 increased the knowledge at the industrial partners about the WCET method to analyse time critical software by carrying out quite a few case studies on industrial software. Furthermore a new version of the WCET tool Bound-T is being developed. WCET has one of the most extensive international co-operation of the ASTEC projects both with the industrial partners (Table 2) and within the EU project ARTIST2. Dr. Xavier Vera defended his thesis in January 2004, he is now at Intel Labs, Barcelona, Spain. Christer Sandberg presented his licentiate thesis in 2005.

The **PLEX** project started in April 2004. PLEX is an in-house language at Ericsson for programming AXE telephone exchanges. Ericsson would like to replace the current, sequential central processor in the AXE with a parallel processor. The existing PLEX code must therefore be parallelised. This requires a formalisation of PLEX semantics for both sequential and parallel execution models. The project has arranged an industrial seminar, made the 2 reports "A Formal Semantics for PLEX" and "Semantics of the language PLEX in a single processor". Johan Lindhult presented his licentiate thesis in 2005. The project is

planned to continue at least until March 2006 with support from Ericsson.

Voices from industry

in 2005 Ericsson AB UKI/O, kenneth.lundin@ericsson.com
"*We have on top of the original plan made a cash contribution of 500 000 SEK since Dialyzer has been such success within the HiPE project and already shown to be valuable for Ericsson.*"

in 2006 Ericsson AB UKI/O, kenneth.lundin@ericsson.com
The research results have been to very big benefit for us. To mentions a few points:

"*Typechecking of Erlang resulted in the Dialyzer tool which now is part of the Erlang/OTP product.*
Dialyzer is used within several development projects within Ericsson and is a very valuable tool in finding error in early phases (before function test) and this saves a significant costs during development.

The bitstring and binary comprehension suggestion (additions to the Erlang language) is very interesting and will be added to the product during 2006.

Many small ideas regarding SMP (Symmetrical Multi-processing) support in the Erlang emulator have sprung from the HiPE group and are now implemented in the product. The SMP support is a real important feature since it allows Erlang programs to take advantage of multi-core technology very easily."

Ericssson AB (michael.williams@ericsson.com)
"*Seen from my perspective, the two contributions from Astec which have gone straight into industrial use (in one way or another) are Hipe and Dializer.*"

TIDORUM AB
The collaboration with ASTEC on development of Tidorum's WCET tool was useful both directly -- much of the work on a tool version for the Renesas H8/300 processor was completed in 2004 -- and indirectly as it exposed the tool's architecture to outside review and comment.

The contact with ASTEC contributed to Tidorum joining the ARTIST2 Network of Excellence, cluster on "Compilers and Timing Analysis" which started in 2004.

The ASTEC/WCET work, in 2004 and currently, on improved modelling of the arithmetic computations in a program (interval analysis, pointer analysis) is very interesting to Tidorum and there is a clear need to add such functionality to Tidorum's WCET tool in the future.
Niklas Holsti, Tidorum Ltd.

6. Participating staff

During phase 4, 85 persons have been directly involved in ASTEC activities (Table 5 and 6), the total activity where 48 man-years (Table 2 in Appendix 1). Note that some persons where involved in several projects.

Table 5. Staff categories

Category	Number of persons
Professor	5
Senior Academic Researcher	7
Industry researcher	37
Industry PhD student	3
PhD student	12
M. Sc. Student	19
Administrative staff	2
Sum	85

Table 6. Staff in each project.

Project	Title *project leader	Name	Affiliation
Admin	Professor	Bengt Jonsson	UU
	Senior Researcher	Kostis Sagonas	UU
	Coordinator	Roland Grönroos	UU
	Economist	Patrik Johansson	UU
AuToWay	Professor	Paul Petterson	UU
	Industry researcher	Tomas Aurell	Ericsson KI/EAB
	Industry researcher	Natalie Jost	Ericsson KI/EAB
	Industry researcher	John Orre	Ericsson KI/EAB
	Industry researcher	Reza Tokhmpash	Ericsson KI/EAB
	Ph.D. Student	Anders Hessel	UU
	M.Sc. student	Joel Dutt	Ericsson KI/EAB
	M.Sc. student	Anna Holmgren	UU
	M.Sc. student	Peyman Tavanaye Rashid	Ericsson KI/EAB
	M.Sc. student	Per Wilhelmsson	Ericsson KI/EAB
DeTrack	Professor	Parosh Abdulla	UU
	Professor	Bengt Jonsson	UU
	Industry researcher	Stig Johansson	WM Data Validation AB
	Industry researcher	Stefan Mangenat	Validation AB
	Industry researcher	Lena Nyberg	WM Data Validation AB
	Industry researcher	Tomas Reidmar	WM Data Validation AB
	Ph.D. Student	Nomene Ben Henda	UU + Validation AB
	Ph.D. Student	Johann Deneux	UU + Prover Technology AB
Fault Tree Analysis	Professor	Parosh Abdulla	UU
	Professor	Bengt Jonsson	UU
	Industry researcher	Ludvig Borgne	Prover Technology AB
	Industry researcher	Gunnar Stålmarck	Prover Technology AB
	Industry researcher	Ove Åkerlund	Prover Technology AB
	Industry Ph.D. Student	Johann Deneux	UU + Prover Technology AB

Table 6. continued.

Project	Title *project leader	Name	Affiliation
HIPE	Senior Researcher	Mikael Petterson	UU
	Senior Researcher	Kostis Sagonas	UU
	Industry researcher	Björn Gustavsson	Ericsson AB (UKI/O)
	Industry researcher	Sean Hinde	T-Mobile Inc.
	Industry researcher	Kenneth Lundin	Ericsson AB (UKI/O)
	Industry researcher	Raimo Niskanen	Ericsson AB (UKI/O)
	Industry researcher	Patrik Nyblom	Ericsson AB (UKI/O)
	Industry researcher	Ulf Wiger	Ericsson AB (UKI/O)
	Ph.D. Student	Per Gustafsson	UU
	Ph.D. Student	Tobias Lindahl	UU
	Ph.D. Student	Jesper Wilhelmsson	UU
	Industry Ph.D. Student	Richard Carlsson	UU
	M.Sc. student	Daniel Luna	UU
	M.Sc. student	Jonas Widjen	UU
PLEX	Professor	Björn Lisper	MDH
	Senior Researcher	Jan Gustafsson	UU/MDH
	Industry researcher	Ole Kjöller	Ericsson AB (APZ)
	Industry researcher	Janet Wennersten	Ericsson AB (APZ)
	Ph.D. Student	Johan Eriksson	MDH
REMODEL	Professor	Björn Lisper	MDH
	Professor	Wang Yi	UU
	Senior Researcher	Anders Wall	MDH
	Industry researcher	Peter Eriksson	ABB Automation Technologies AB
	Industry researcher	Magnus Larsson	ABB Automation Technologies AB
	Industry researcher	Christer Norström	ABB Automation Technologies AB + MDH
	Ph.D. Student	Pavel Krcal	UU
	Ph.D. Student	Leonid Mokrushin	UU
	Ph.D. Student	Shi XiaoChun	UU
	Industry Ph.D. Student	Johan Andersson	ABB Automation Technologies AB + MDH
	M.Sc. student	Irobi Ijeoma Sandra	MdH
	M.Sc. student	Anders Johnsson	MDH
	M.Sc. student	Roy Nilsson	MdH
SAAPP	Senior Researcher	Björn Victor	UU
	Industry researcher	Jakob Engblom	Virtutech AB
	Industry researcher	Bengt Verner	Virtutech AB
	Ph.D. Student	Karl Marklund	UU
STEP	Professor	Bengt Jonsson	UU
	Professor	Paul Petterson	UU
	Industry researcher	Göran Båge	MobileArts AB
	Industry researcher	Lars Kari	MobileArts AB
	Industry Ph.D. Student	Johan Blom	MobileArts AB + UU
WCET	Professor	Björn Lisper	MDH
	Senior Researcher	Andreas Ermedahl	UU
	Senior Researcher	Jan Gustafsson	MDH
	Industry researcher	Christian Ferdinand	AbsInt Angewandte Informatik GmbH
	Industry researcher	Jörgen Hansson	CC-systems AB
	Industry researcher	Niklas Holsti	Tidorum AB

Table 6. Continued.

Project	Title *project leader	Name	Affiliation
WCET continued	Industry researcher	Anders Kallerdahl	Volcano Communicaton Technologies AB/Mentor Graphics AB
	Industry researcher	Jan Lindblad	ENEA Embedded Technology AB
	Industry researcher	Ken Lindfors	CC-systems AB
	Industry researcher	Kurt-Lennart Lundbäck	Arcticus Systems AB
	Ph.D. Student	Christer Sandberg	MDH
	M.Sc. student	Stefan Bygde	MDH
	M.Sc. student	Susanna Byhlin	MDH
	M.Sc. student	Ola Eriksson	MDH
	M.Sc. student	Samuel Petersson	MDH
	M.Sc. student	Daniel Sandell	MDH
	M.Sc. student	Daniel Sehlberg	MDH
	M.Sc. student	Yina Zhang	MDH
WPO	Senior Researcher	Sven-Olof Nyström	UU
	Industry researcher	Jan-Erik Dahlin	IAR AB
	Industry researcher	Mats Fors	IAR AB
	Industry researcher	Olle Landström	IAR AB
	Industry researcher	Carl von Platen	IAR AB
	Industry Ph.D. Student	Johan Runesson	UU + IAR AB
	M.Sc. student	Andreas Lundin	UU
	M.Sc. student	Henrik Nyman	UU
	M.Sc. student	Daniel Widenfalk	UU

7. Economy report

The total industrial contribution reached 16 250 693 SEK, 118% of the planned amount (Tab 7 and 8). Most of the activities were carried out as planned. A few changes worth mentioning is the increased interest by Ericsson AB in the HiPE project that resulted in increased efforts and also in cash contributions to ASTEC. A few industrial partners changed owners (IAR Systems AB were bought by NOCOM AB), Validation AB by WM-Data and Volcano Communication Technologies AB by Mentor Graphics (Scandinavia) AB. These changes led to new focus in these partners. EuroControl were not able to sign the agreement due to their juridical construction.

Table 7. Budget and result for phase 4

	Budget (SEK)	Division (%)	Result (SEK)	Division (%)
Industry*	13 804 000	37%	16 250 693	38%
Academia (Uppsala and Mälardalen Universities)	10 000 000	27%	12 595 021	29%
VINNOVA**	13 906 475	37%	14 133 915	33%
Sum	37 710 475	100%	42 979 629	100%

* A few industrial partners were not able to join ASTEC. Their planned contributions have been omitted from the budget and result even though some studies were carried out.

** VINNOVA contribution transferred from phase 3 (1906 475 SEK) is included in budget. Result includes interest, which explain a slightly higher result than budget.

Table 8. Industrial contributions phase 4

	Budget	Result		
Industry	(SEK)	Total (SEK)	Cash (SEK)	% of budget
ABB Automation Technologies AB	2 000 000	2 020 200	600 000	101
AbsInt Angewandte Informatik GmbH	2 530 000	2 013 035	-	80
Arcticus Systems AB	100 000	100 400	-	100
Cross Country Systems AB	40 000	126 000	-	315
ENEA Embedded Technology AB	250 000	344 040	-	138
Ericsson AB (APZ, UKI/O, KI/EAB)	3 592 000	4 930 640	1 483 000	137
~~EuroControl~~	~~629 000~~			
I.A.R. Systems AB	500 000	694 500	-	139
Mobile Arts AB	1 000 000	1 000 000	-	100
Prover Technology AB	2 000 000	3 468 000	-	173
~~T-Mobile (UK) Ltd.*~~	~~500 000~~	-	-	0
TIDORUM AB	610 000	557 578	-	91
Virtutech AB	832 000	811 500	-	98
~~Voleano Communicaton Technologies AB~~	~~720 000~~	-	-	0
Volvo Teknisk Utveckling AB	50 000	-	-	0
WM data Validation AB	300 000	184 800	100 000	62
Sum	**13 804 000**	**16 250 693**	**2 183 000**	**118**

8. Information activities

Our website www.astec.uu.se is available with information about publications, reports and open software developed within the projects etc. Most of the 259 publications are available via the ASTEC website.

9. Plan for activities after the ten years of VINNOVA funding.

ASTEC laid the foundation for the excellent university reviews the Department of Information Technology obtained in 2007. At Mälardalen University is the heritage of ASTEC further developed within the SSF funded centre PROGRESS. We continue the process to expand the co-operation between industry and academia.

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2007-07-08

ASTEC
Advanced Software Technology

Appendix 1.

Final presentation of business ratios for ASTEC 1995 - 2007[1]

One of the criteria for a successful competence centre is expansion. As seen from the following graphs and tables ASTEC increased its activities in many aspects over the first years. ASTEC were also capable to continue its level of activities during the crisis in the IT-sector during 2001-2003. This was partly achieved by increasing the number of industry partners (Fig 1). Expansion started again as times become well in 2004. Even the last year of activities 2005 increased the industry participation (Fig 2).

The industrial partners could not contribute according to the plan for phase 3. As a result of the restrictions in the agreement was the VINNOVA contribution decreased during 2003 (Fig 2, Tab 1). This had the effect that some VINNOVA funding was transferred into phase 4 (2004 and 2005). To maintain the staff had the academia to increase its contributions during 2002 and 2003. An intensive effort to broaden the industrial base for phase 4 were successful both the number of industrial parts (Fig 3) and their contributions during Phase 4 (Fig 2, Tab 1). The amount of studies and work carried out within ASTEC increased 2000 and 2004 (Fig 3) this is partly explained by increased number of MSc studies these years (Tab 2).

The costs for each man-year were 866 KSEK and the costs for management were 6.6% on average for the 10 years (Tab 1). In total has ASTEC carried out 179 man-years of studies (Tab 1).

ASTEC produced 259 publications, in these publications have 169 authors contributed (Fig 4, Tab 3). The publication rate dropped slightly at the start of each phase. This happens since it takes a while for new projects to obtain publishable results. This phenomenon can be seen at 1995, 1998, 2001 and 2004. The increased cost per publication and time requirement per publication also reflects the start of phases 1, 2 and 3 (Tab 1, Figs 5 and 6).

Roland Grönroos

[1] ASTEC business ratios are calculated from the costs and activities each year. There is no profit within ASTEC. Contributions from the parts are consumed the same year. The research results are transferred to the participating companies that may profit from them and according to the contracts share the profit with the researchers.

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SE-751 05 Uppsala, Sweden	Lägerhyddsvägen 2, Uppsala	+46 18 471 3157		http://www.astec.uu.se/

Figure 1) Number of industry partners in ASTEC 1996-2005.

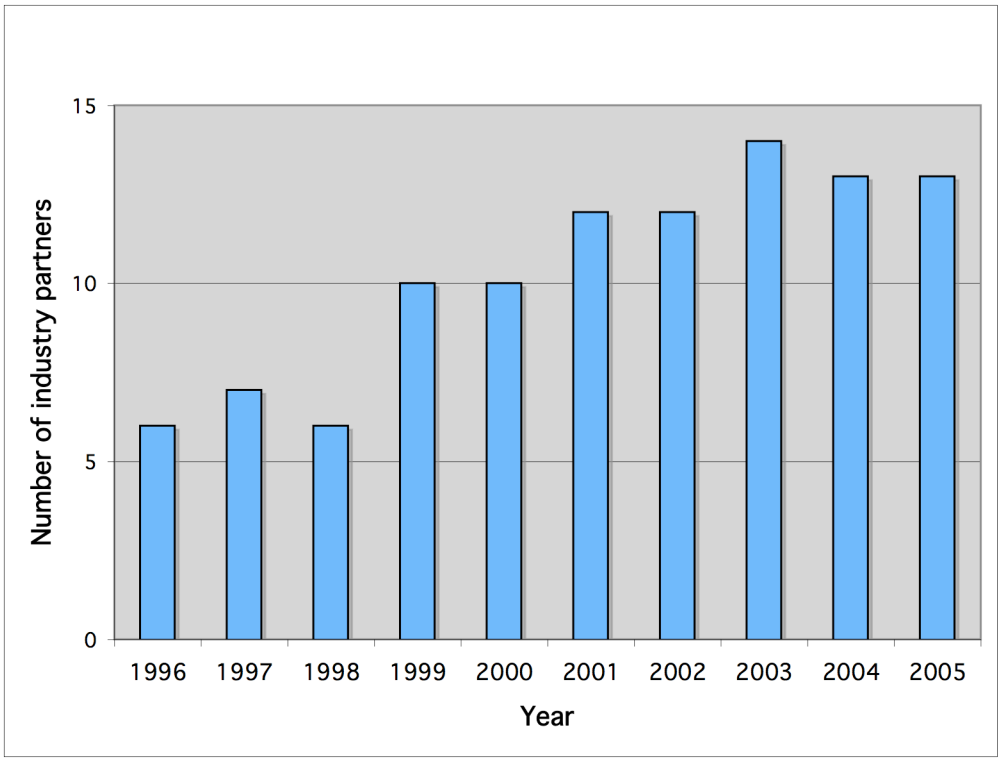


Figure 2) The yearly contributions to ASTEC by NUTEK/VINNOVA, Academia and Industry.

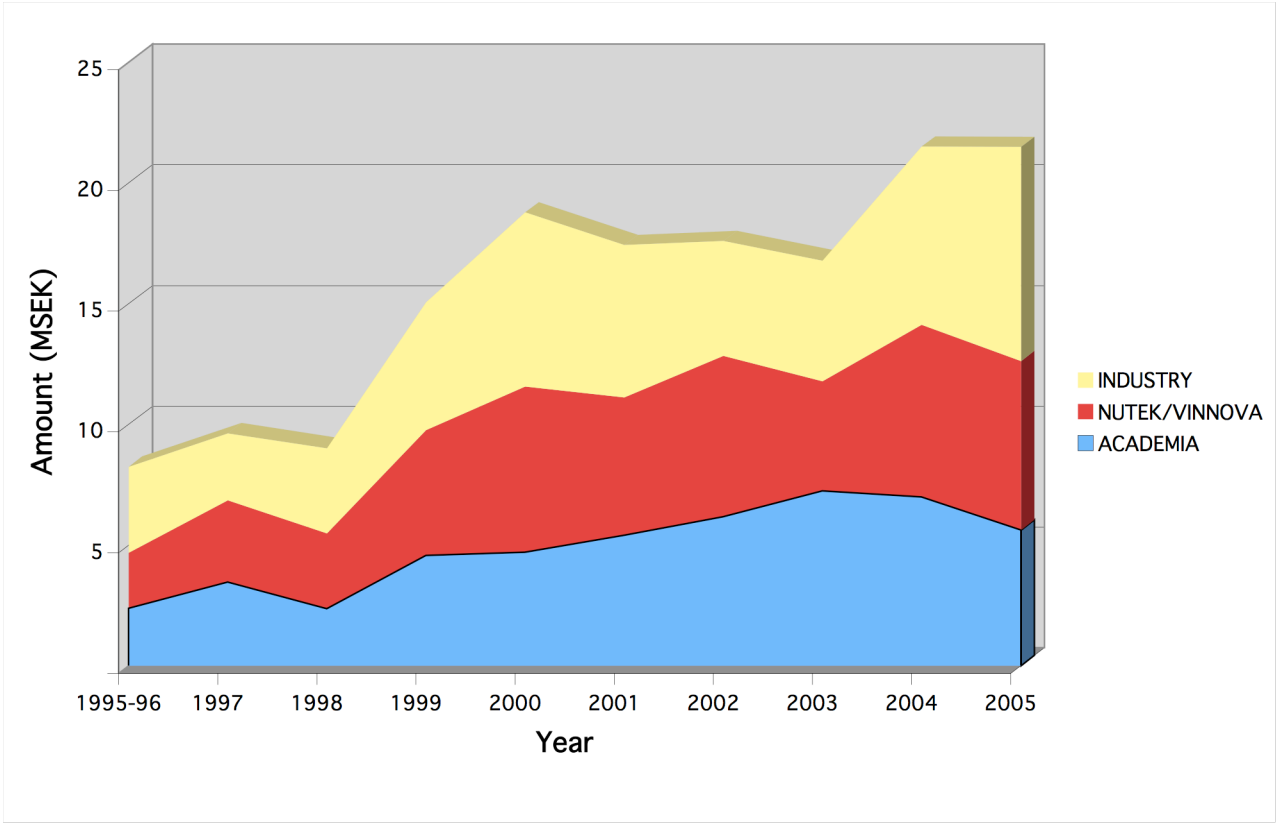


Figure 3) The amount of studies carried out within ASTEC in man years for each year.

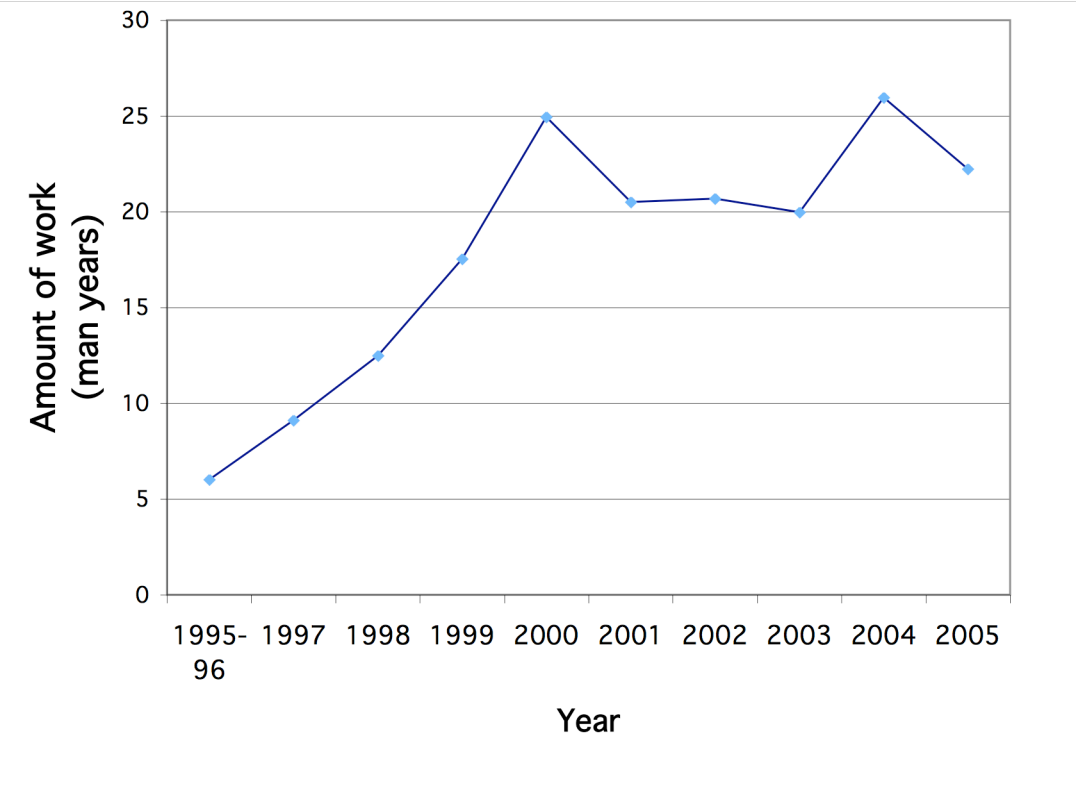


Table 1) The contributions by ASTEC partners and business ratios.

	Phase 1			Phase 2		Phase 3			Phase 4		
	Year										
Contributions by	**1995-96**	**1997**	**1998**	**1999**	**2000**	**2001**	**2002**	**2003**	**2004**	**2005**	**Sum**
INDUSTRY	3568	2778	3520	5293	7219	6317	4759	5000	7385	8866	54705
ACADEMY	2375	3450	2347	4557	4688	5392	6159	7240	6982	5613	48804
NUTEK/VINNOVA	2295	3395	3134	5202	6869	5712	6672	4534	7128	7006	51948
Total (KSEK)	8238	9623	9001	15053	18777	17421	17591	16773	21495	21485	155456
Management (KSEK)	380	818	721	1038	1066	1336	1293	1275	1180	1158	10264
Man power(man years)	6,0	9,1	12,5	17,5	25,0	20,5	20,7	20,0	26,0	22,2	179
Publications (no.)	8	19	12	22	35	28	33	34	29	28	248
											Mean
KSEK/man year	1371	1054	719	858	753	849	851	839	828	968	866
KSEK/Publication	1030	506	750	684	536	622	533	493	741	767	627
Man years/publication	0,75	0,48	1,04	0,80	0,71	0,73	0,63	0,59	0,90	0,79	0,72
Management/Total	5%	9%	8%	7%	6%	8%	7%	8%	5%	5%	6,6%

Table 2) Development of ASTEC staff categories,.

	Amount each year (man years)									
Category	**1995-1996**	**1997**	**1998**	**1999**	**2000**	**2001**	**2002**	**2003**	**2004**	**2005**
Professor	0,5	0,3	0,6	0,6	2,1	1,8	1,4	1,3	1,3	1,0
Senior researcher	1,2	2,1	2,5	4,1	2,8	2,4	2,1	2,1	2,9	2,5
PhD student	3,3	4,1	6,3	7,1	9,0	7,1	10,6	8,3	8,4	8,5
Industry researcher	1,0	1,7	2,2	2,1	3,8	1,7	2,5	2,8	3,5	3,1
Industry PhD students				2,0	3,0	4,0	1,9	3,1	4,1	2,1
Master of Science students				1,0	3,9	3,2	1,9	2,1	5,5	4,6
Technical/administrative		1,1	1,0	0,6	0,5	0,4	0,3	0,3	0,3	0,5
Total=	6,0	9,1	12,5	17,5	25,0	20,5	20,7	20,0	26,0	22,2
Increase each year (man years)	-	3,1	3,4	5,0	7,4	-4,4	0,2	-0,7	6,0	-3,7
Increase each year (%)	-	52%	37%	40%	42%	-18%	1%	-3%	30%	-14%

Publications and exams

Figure 4) Publication rate and type of publication.

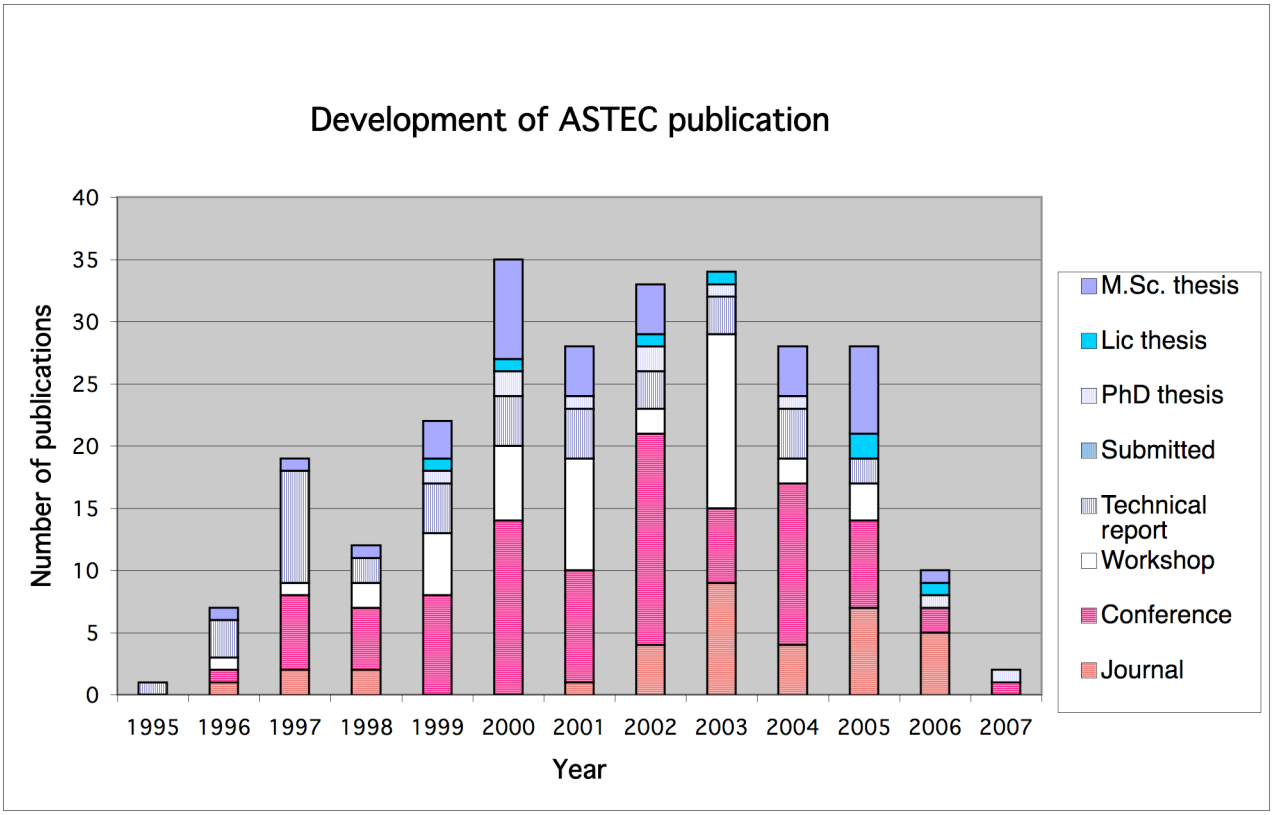


Table 3) Publication divided into different publication categories, note that conference, workshop and technical reports are dominating.

Publications type	year													Sum
	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	
Journal		1	2	2			1	4	9	4	7	5		35
Conference		1	6	5	8	14	9	17	6	13	7	2	1	89
Workshop		1	1	2	5	6	9	2	14	2	3			45
Technical report	1	3	9	2	4	4	4	3	3	4	2			39
Submitted														0
PhD thesis					1	2	1	2	1	1		1	1	10
Lic thesis					1	1		1	1		2	1		7
M.Sc. thesis		1	1	1	3	8	4	4		4	7	1		34
Sum	1	7	19	12	22	35	28	33	34	28	28	10	2	259

Figure 5) Time requirement per ASTEC publication, note the decrease in time per publication as a new phase develops. Phase 1 started 1995, phase 2 started 1998, phase 3 2001 and phase 4 in 2004.

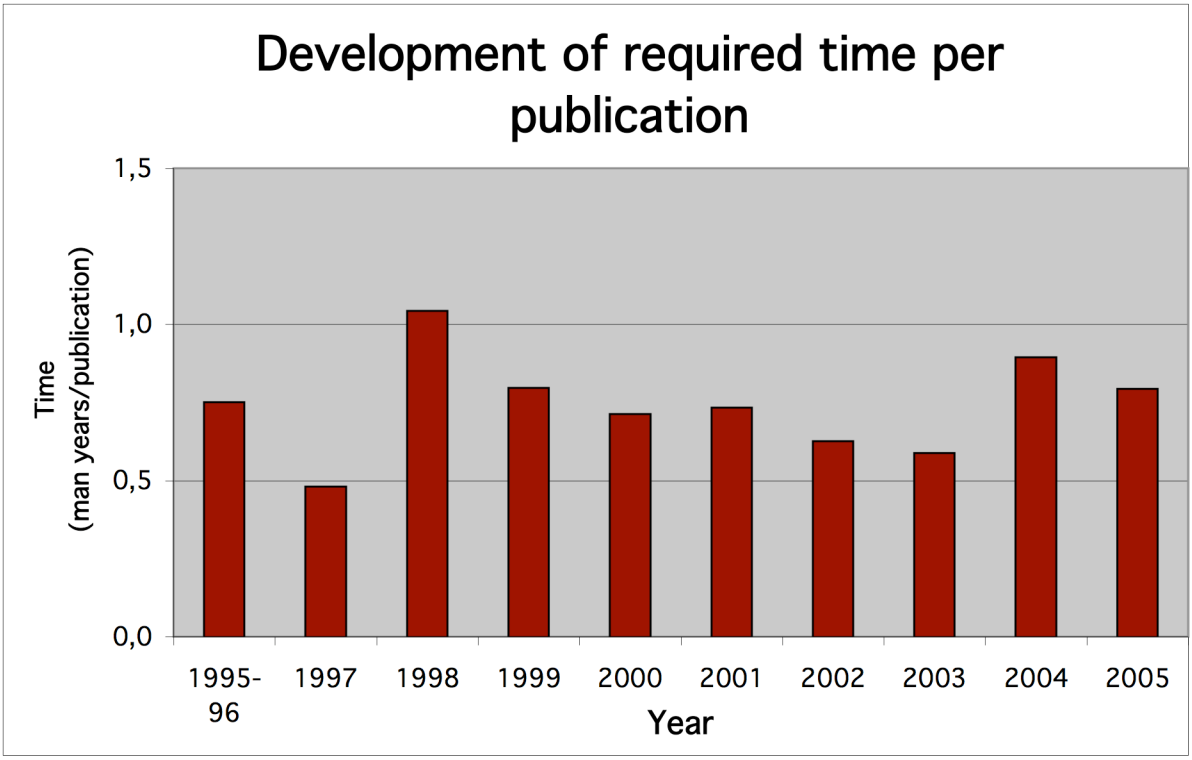
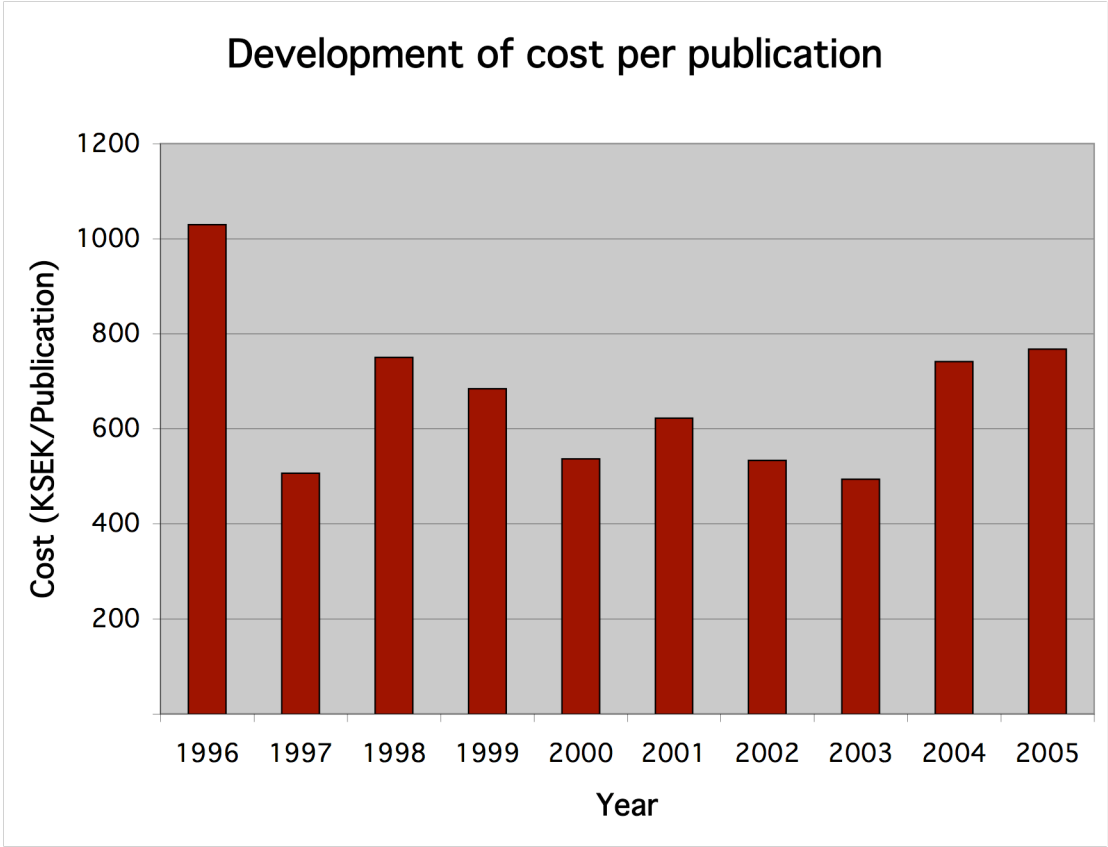


Figure 6) The cost per ASTEC publication, note a similar trend as in the previous figure.



Review - ASTEC Scientific Advisory Day: September 14th , 2004

These remarks expand on the verbal summary made on Sept. 14th by the ASTEC Scientific Advisory Board comprising of Neil Jones (University of Copenhagen), Bernhard Steffen (University of Dortmund) and Neeraj Suri (TU Darmstadt).

As ASTEC is entering its last year of operation, the nature of our comments differs from past reports. In this instance our comments are more oriented towards minor re-tuning (perhaps for financial allocation of remaining ASTEC funding) of projects, as well as offering some suggestions for conducting a reflective assessment of ASTEC accomplishments over its tenure.

Some brief comments on the individual projects - we refrain from detailed technical comments given the stage of development of the projects.

AUTOWAY: Syntax free, model based, timed specs environment and generation of test sequences is both a technologically challenging and high applied-impact project (Ericsson WAP Gateway). This project has developed really well and sustained effort for it over the duration of ASTEC (and beyond it) would be a very worthy endeavor. The co-development of the formal constructs for test criteria and associated tool development is a solid effort worth completing, and further development and generalization.

STEP: Specification Testing Env. for Erlang Protocol SW: For STEP, we express a positive tenor similar to AUTOWAY. Generalizing to non-Erlang specific protocols would be a useful thrust to develop.

DETRACK: Given the changes in industrial support for this project, perhaps this project may need to be de-scoped. It might be worth considering how the current processes for ascertaining input - output correlations might be useful for the other ASTEC testing projects.

WCET: This project has really matured. In the past, we have expressed critiques about the fuzzy plan for end-goals for this project. At this stage, we find the accomplishments and clear focus on automated flow analysis, static analysis for dynamic program behavior, and the technology transfer projects (ENEA, Volcano, Bound T) to be very meaningfully set up. This project would benefit from sustained support. WCET ties to ongoing EU activities such as ARTIST2 should provide a continued forum for its impact on the community.

REMODEL: Simulation based timing analysis of industrial RT systems: Another solid project worth supporting fully .

HIPE has always been quality work and this is continuing well. The development of the DIALYZER automated code "deficiency/inconsistency/anomaly" highlighting tool is an excellent industrial impact effort that could be expanded. Aspects of automation, degree of

false warning vs. coverage issues, nature of deficiency, and tying detection to design process all offer interesting growth areas.

PLEX: Parallel Execution of PLEX programs - While we appreciate the strong industrial need from Ericsson for PLEX, its generalized impact (academic and technical) is limited and unclear at present. Additional efforts scoping its potential to general code transformation/parallelization aspects would be helpful. The presented relation (constraint?) to OO methodologies was not convincing. Perhaps, industrial support offers the more relevant support forum for PLEX.

Safety Analysis: Fault Tree analysis with SCADE: There is much existing work in this area since the 70's. It would help to have a crisper relation shown to existing state of the art, criteria for evaluating success, and the potential for future impact in ASTEC and outside, prior to scoping future efforts for the project.

SAAPP: Simulator Aided Analysis of Parallel Processes: A prototype based on the Virtutech SIMICS system has been developed, but it was unclear whether Virtutech is participating in the research. The presentation seemed only to describe application of ideas known from RecPlay, and no SAAP-authored reports appeared in the reference list beyond mention of a planned NWPT'04 paper. The project's goals and success criteria were less convincing than some of the other ASTEC projects. In our opinion they need considerable sharpening if SAAPP is to continue into ASTEC's final period.

WPO: Whole Compiler Optimization: While reasonable work has been done here, and a workshop paper presented, it looks like a point of diminishing returns has been reached. WPOs stated goal is "not to discover new techniques but to discover whether standard, rather labor-intensive techniques can be replaced by simpler ones". The scientific value of this is unclear, as well as the question of just how it could be proved/disproved. Also unclear is the amount of IAR participation in the scientifically relevant part of the project, and the relevance of the C++ cross compiler.

General Suggestions:

Planning for the coming year, we suggest sustained support for AUTOWAY, STEP, WCET, REMODEL and HIPE. The projects with higher applied content might be better expanded with industrial support as appropriate.

It might be a useful ASTEC internal assessment, and also for future planning activity, to consider some form of tabulation of all project results. Some possibilities might be to tabulate along the following lines:

1. Overall Planned Goal
2. Scientific Plans
   a) Planned Scientific Goals

b) Derivate Scientific Goals (planned or resultant from project progress)

3. Scientific State of the Art
4. Status of Achieved Results: Success Metrics
   - fundamental advancements?
   - impact?
   - leading to other open problems?
5. Status of project:
   - done?
   - modified?
   - sets the foundation for future larger problems?

6.. Identically for Applied/Technology Transfer/Tools and plans
   a) ...
   b) ...

This might help crystallize all key ASTEC contributions and also help in planning for the future.

Overall, we emphatically feel that ASTEC has developed over the years to be considered a success story for a competence center. Its development of competence in SW within Sweden is undisputed, and has made its mark as a leading center worldwide! Given its academic and applied impact, we strongly support any efforts that would help sustain (& increase) the essence of this competence for the years ahead.

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Advanced Software Technology

ASTEC (Advanced Software TEChnology) is a competence center in the area of software technology. Its purpose is to develop and support industrially applicable techniques for software specification, design, and development. It shall bring new technlogy into industrial applications and perform academic research on industrially relevant problems in software development. High-level specification and programming languages, together with tools for specification, analysis, validation, simulation, and compilation are central topics of the center. Particular emphasis is put on methods supporting the development of software for communication and control applications.

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   - Ericsson AB (the departments APZ, UKI/O and KI/EAB)
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