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ASTEC
Advanced Software Technology

ASTEC

Advanced Software Technology

This document is the

Report for year 6

the first year in phase 3

The year 2001.

Uppsala April, 2002

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Director

Up-to-date information about current activities can be found on the
WWW page http://www.astec.uu.se/

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Summary

The main results of ASTEC during year 6.

1. At the initiation of Phase 3, the number of companites increase from 10 to 12.
2. During 2001, 28 publications, one Ph.D. and 4 M.Sc. degrees have been completed.
3. Information dissemination efforts have increased in the form of seminars and survey presentations at conferences.
4. Several graduate seminars have been conducted.
5. Three projects have been concluded during 2001. Results have been delivered to industry, and included into graduate education.
6. Four new projects are starting.
7. The involvement by MdH has increased, mainly due to a significant expansion of the WCET (Worst Caes Execution Time) project.
8. The HIPE (High Performance Erlang) compiler has been incorporated into the open source distribution of Erlang.
9. The general decline in the IT area is reflected in ASTEC business ratios.
10. The direct and indirect involvment of ASTEC into research under the auspicies of the EU is increasing. ASTEC has been instrumental in developing a basis for participation in European Research Networks.

Sammanfattning

De viktigaste resultaten av ASTEC under år 6.

- Från fas 2 till fas 3 has antalet näringslivsintressenter ökat från 10 till 12.
- Under 2001 har 28 publikationer, en doktordisputation och fyra examensarbeten avklarats.
- Informationsspridningen har ökat genom att flera seminarieserier hållits och genom översiktliga presentationer på konferenser.
- Flera doktorandkurser har hållits.
- Tre projekt har avslutatas under året, resultaten har levererats till industri och inlämmats i undervisningen.
- Fyra nya projekt har startats.
- Samarbetet med Mälardalenshögskola har ökat främst genom en kraftig ökning av WCET (Worst Case Execution Time) projektet.
- HiPE compliern har inlämmats fullt ut i open source Erlang.
- Den övergripande nedgången inom IT sektorn avspeglas även i ASTEC:s nyckeltal.
- Engagemanget i EU-projekt ökar kontinuerligt, förnärvarande är ASTEC indirekt med i ett projket med syfte att förbereda en ansökan till 6:te ramprogrammet. ASTEC har medverkat till att utveckla en bas för deltagande i Europeiska forskarnätverk.

Contents

Introduction

ASTEC (Advanced Software Technology) is a competence centre which focuses on Advanced Tools and Techniques for Software Development. Development of software accounts for a significant part of the costs in the construction of a number of important products, such as communication systems, transportation and process control systems, of Swedish industry. It is thus a vital interest to be able to produce better software at lower cost. One of the means to achieve this is to improve the tools and techniques used for software development. ASTECs vision is that, wherever possible, software should be developed using high-level specification and programming languages, supported by powerful automated tools that assist in specification, analysis, validation, simulation, and compilation. The purpose of ASTEC is to conduct pre-competitive and industrially applicable research that contributes to this vision, to build up and offer a concentrated research environment in the software technology area, and to be a forum for contacts and exchange of ideas between academia and industry.

ASTEC has been formed as a consortium of academic partners with strong research programs in different areas of software technologies, and of companies which either have a substantial

software production or produce tools for software development. During the first two years, the focus of ASTEC was to connect academia with industry by conducting projects where techniques from academia were applied to problems in industry. This phase created a network of contacts between academia and industry. After the initial phase, a strategic perspective for the long-term development of ASTEC was added, which has led to a focus and build-up of effort in key strategic areas.

Currently, ASTEC has developed into a focussed and distinct research unit, having a broad contact area with a number of companies. It is a natural forum for collaboration, discussions, and new contacts in the software technology area.

Partners

ASTEC has been formed as a consortium of the following academic and industrial partners during phase 3.

- Research groups at *Uppsala University*, the *Swedish Institute of Computer Science* (SICS), and *Mälardalen University*, working mainly on formal methods, functional, logic and constraint programming, compilation, and on embedded, distributed, and real-time systems, together with
- companies with a substantial software production and thus a large interest in software development. These include companies: *ABB Automation Products AB, Cross Country Systems AB, Ericsson Utvecklings AB, ESAB Welding Equipment AB, Validation AB, and Volvo Teknisk Utveckling AB,* and
- companies that produce tools for software development: *ENEA Ose Systems AB, IAR Systems AB*, *Prover Technology AB*, *Telelogic Sverige AB*, *Virtutech AB*, and *Volcano Communication Technologies AB*.

General Observations

In the transition from Phase 2 to Phase 3, the following general points are notable.

- There has been a shift in technical focus of several projects, especially within the Validation and Verification area. Compared to Phase 2, there is In Phase 3 is less emphasis on formal verification, whereas more attention is paid to other verification techniques, such as testing, program analysis, and simulation. In addition, new activites on code generation and scheduling are starting.
- The level of activities during 2001 is lower than during 2000, including delays in starting up new projects. This is due to a combination of the general decline in the IT-area, and difficulties in recruitment during 2001. These problems (in particular the latter) are expected to vanish during 2002.
- Results of ASTEC work has been disseminated for industrial usage. This includes the HIPE compiler, which has been incorporated into the open source release of Erlang as of September 2001.

General Figures

During 2001, 28 publications, including 1 Ph.D. thesis and 4 M.Sc. theses have been produced (see Appendices 1 and 2). Within the ASTEC seminar series, 25 seminars were given (Appendix 4). A comparison with previous years is given in Appendix 3.

Research Activities

Concluded Projects

Several projects have been concluded at the beginning of phase 3.

- The Project **Erlang Verification**, which develops a tool for formal verification of Erlang programs, has been concluded as of summer 2001, by a delivery and demonstration at Ericsson, and by the completion of Lars-åke Fredlund's Ph.D. thesis.
- The Project **Static Analysis** has been concluded by a seminar, and by incorporation of results into graduate courses given during 2001.
- The Project **Auto** has been concluded at the end of Phase 2. The last result is a major case study, in which a car locking system has been modeled and analyzed using the UPPAAL tool. Mecel AB has left the ASTEC consortium at the end of Phase 2.
- The Project **BUS**, in which an industrial bus protocol has been modeled and analyzed using UPPAAL, has been concluded with an evaluation by ABB. The insights from the BUS project will guide future projects that aim at investigating how to use formal verification technology in industrial software development.

The projects on formal verification have exhibited possibilities and bottle-necks for the application of formal verification within industrial software development. Guided by insights from these projects, new activities are starting, as described in the next paragraph.

New Projects

Guide by the experiences of previous projects, and by comments made in the evaluation, new projects have been initiated, especially within the area of Verification and Validation.

- The project **Erlang Analysis** develops techniques and a tool for extracting the process structure of Erlang Systems from source code. The extracted process structure is analyzed in order to detect potential problems in recovering from failures. The project will conclude by Autumn 2002 with the Ph.D. thesis of Jan Nyström.
- The project **Simulator-Aided Analysis of Parallel Processes**, in collaboration between UU and Virtutech AB, develops techniques for simulation of parallel programs in order to detect concurrency problems. The project is based on the the SIMICS simulator for multiprocessor systems. Due to difficulties in recruitment during 2001, the actual starting date is April 2002.
- The goal of project **Software Synthesis** is to develop a tool, called TIMES, for generating code for distributed embedded systems, starting from a high-level specification, by means of scheduling and code generation. A C-code generator has been developed for the LegoOS.

- The purpose of the project **TAS: Time-Accurate Simulation of Distributed Embedded Real-Time Systems** is to add mechanisms to enable simulations of Distributed Embedded Systems to be performed in actual real-time on a powerful workstation or PC. The approach is to analyze actual execution times of code segments, and use timers to control the scheduling of processes on the workstation.

Other significant new activities are:

- In connection with the project Software Synthesis, M.Sc. projects in collaboration between UU and ABB, are investigating how to use formal verification technology in industrial software development. The M.Sc. projects are supported by a seminar series.
- In connection with the project on Erlang Verification, Ericsson UA has developed tools for generating models from Erlang programs which are subject to model checking. In a recently concluded project, techniques for visualizing and analysing traces generated during execution of Erlang Programs have been developed.
- The project on testing has been expanded by a Ph.D. student, and by associating one more senior researcher. During winter 01/02, a seminar series in the area is being conducted.
- Several M.Sc. projects have been conducted in connection with the project Worst Case Execution Time Analysis, with the aim of evaluating the potential benefits and bottlenecks when applying WCET technology.

Change in Project Focus

The project SMC, which develops techniques for using satisfiability checking in system verification, has previously focussed on using satisfiability checking as a tool in model checking of hardware designs. During 2001, the focus has shifted to analysis of fault trees, and how satisfiability checking can be used for this problem.

Industrial Exploitation

ASTEC is on its way to make research results industrially exploitable.

- The **HiPE (High Performance Erlang)** compiler has been incorporated in the open source distribution of Erlang. This major goal of the project was achieved in two steps: First, HiPE was ported to the latest OSE implementation (Release 7B-1). This step was completed in February 2001. Since then, a much closer co-operation between the HiPE team and the Erlang/OTP team from Ericsson was established through very frequent (almost twice a week) exchange of code snapshots and through regular day-long meetings once every two months. This has resulted in incorporating HiPE into the main branch of the Erlang development and HiPE was finally released as part of Erlang/OTP Release 8B in October 2001.
  Experience from using HiPE is so far positive. At least judging from postings to the Erlang mailing list, HiPE is used by a number of Erlang programmers. The development team of Erlang at Ericsson Utvecklings AB is extremely interested in HiPE and is even considering including support for HiPE in the commercial release of Erlang/OTP planned for the fall of 2002.
- A **back-end of HiPE for the Intel x86 architecture**, which is an important development platform these days, was designed and developed. A lot of effort was put so that this port

reached the level of maturity and robustness that is expected from an industrial-strength Erlang compiler. Results show that the resulting system, HiPE/x86, is significantly faster than the Ericsson implementation of Erlang, and achives speedups comparable to and sometimes better than those of the more mature HiPE/SPARC compiler. This compiler is also included in Erlang/OTP Release 8B, and is used by the Erlang community.

- The WCET project has conducted several case studies, with the aim of evaluating the usefulness of WCET technology for industrial applications. There are currently discussions to develop a commercial WCET tool, in collaboration between IAR Systems AB, and a small Finnish company.
- At CC-systems, Magnus Nilsson implemented a prototype of a system for time-accurate simulation of embedded systems on a PC, which has been taken into production use.

Collaboration

Within ASTEC

The projects WPO (Whole Program Analysis), WCET (Worst Case Execution Time) and TAS (Time Accurate Simulation) are conducted in close collaboration within the CODER project (or cluster project), which engages at least 4 companies. The collaboration concerns infrastructure for a C compiler, joint organization of graduate courses, and joint project meetings. The projects are planned to be merged in the future, and discussions are underway to associate the Software Synthesis project.

National Collaboration

The national research programme ARTES which supports research and promotes graduate education, hosted at Uppsala University and funded by SSF (The Swedish Foundation for Strategic Research) with a budget of 88MSEK during 1998-2002, was initiated in 1998 with the support and involvement of several ASTEC researchers. Currently, Prof. Hans Hansson is program director, and he and Parosh Abdulla and Wang Yi conduct projects funded by ARTES. There is a close coordination between ASTEC and ARTES work: the two bodies share Roland Grönroos as administrator, and several ASTEC projects are closely related to ARTES projects.

International Collaboration

- **OFFIS, Univ. of Oldenburg (Germany)**
  During Autumn 2001, ASTEC has been hosting Prof. Werner Damm, Univ. of Oldenburg, as a guest professor (visit supported mainly by STINT). Prof. Werner Damm is director OFFIS, an institute for academic-industrial collaboration projects, in areas largely overlapping with ASTECs, and employing over 30 researchers. During the visit, Prof. Damm gave a graduate seminar series on RT-UML and Safety Critical Systems.
- **C-lab, Paderborn (Germany)**
  The WCET project has been in close collaboration with Friedhelm Stappert, at C-Lab in Paderborn, resulting in two "work in progress" papers at RTSS'00 and a publication at CASES 2001.
- **Seoul National University (SNU), Korea**
  Andreas Ermedahl (WCET project) spent Aug. 2000 - Jan. 2001 at SNU. He mainly worked on modeling of energy consumption of embedded processors, resulting (so far) in

a publication. C-Lab in Paderborn, resulting in two "work in progress" papers at RTSS'00 and a publication at CASES 2001.

- The collaboration with **RWTH Aachen**, mainly with researchers at SICS, has been further developed.

All the above international collaborations are expected to continue.

Graduate Education

ASTEC has been organizing the following graduate seminars/courses

- A course on program analysis, focussing on techniques for analyzing pointers, aliasing, and other similar program properties.
- A seminar series on RT-UML and Safety Critical Systems, given by visiting professor Werner Damm, OFFIS, Oldenburg.
- A graduate level programming language implementation seminar focussing on just-in-time compilation and memory management of high-level languages.

Dissemination

- **Industry Presentations**
  At IAR Systems, Jakob Engblom has created an industry presentation named “Getting the Least out of Your C Compiler”. It deals with how to write good C code that generates the smallest possible object code. The premiere was at the Embedded Systems Conference in San Francisco in April 2001, and a sneak preview was given at the Embedded Seminar in Kista in January 2001 (with very good reviews from the audience and in an article in Elektroniktidningen). Further instances have been presented at the Microchip MASTERS conference in Phoenix in July 2001, and the Embedded Systems Conference in Stuttgart in October 2001. The presentation also formed the base for a new course from IAR Education: “A C Refresher for Embedded Programmers”, which is being sold to IAR customers (with Jakob as the teacher). It was given at an Ericsson unit in Lysekil in February, and internally at IAR in Jönköping in March. A group from a DSP processor design group at Ericsson Radio Access in Kista visited Uppsala in October 2001 and was given a lecture about WCET analysis. There is some hope for a future collaboration with this group. The contact resulted from Jakob being the examiner for a master’s project at Ericsson.
- **In the Press**
  Andreas and Jakob were interviewed by Elektroniktidningen, resulting in a full-page article on how to optimize software and hardware architectures for reduced power consumption. Jakob was featured as an example of a well-funded PhD student in a University special published by Uppsala Nya Tidning, contrasted with the poor funding situation at the Theology department. Jakob has started publishing a series of short articles on how to write better C Code on the website of IAR Systems, and in IAR Systems’ customer magazine, “Programming Micros”.
- **Evangelization about WCET**
  Jakob has presented WCET analysis for one IAR customer, and will give lectures on WCET analysis at Chalmers and KTH in February 2002. Jakob and Andreas have prepared a popular presentation of WCET analysis for the ARTES popular writing

competition. Andreas has also created a poster about WCET research as part of a course in communication with non-scientists.

Strategies for Long Term Development

The direct and indirect involvment of ASTEC into research under the auspicies of the EU is increasing. ASTEC has been instrumental in developing a basis for participation in European Research Networks.

- The WOODDES (Workbench for Object Oriented Design and Development of Embedded Systems) project is devoted to development technology for embedded systems in automotive and telecommunication industry within the framework of UML. The project has 6 industrial partners, representing European automotive industry, telecommunication and tools developers and 2 academic partners: Oldenburg University, Germany and Uppsala University.
- The European VERIFICARD project will study security aspects of the JavaCard programming platform for Smartcards, by means of software verification techniques. A contribution will be to adapt our work on compositional proof techniques developed within ASTEC.
- The ADVANCE project "Advanced Validation for Telecommunication Protocols", will develop tools that extend the power of formal analysis. Its partners include Uppsala and Ericsson. Our participation in all these projects builds directly on ASTEC work.
- UU and MdH have engaged in the preparation for the 6th Framework Programme, by participating in the ARTIST Initiative. ARTIST (Advanced Real Time Systems in IST) brings together around 20 strong research groups in Europe in the area of Advanced Real Time Systems. The objective of ARTIST is to
  - Improve awareness of academics and industry in the area, especially about existing innovative results and technologies, standards and regulations.
  - Define innovative and relevant work directions, identify obstacles to scientific and technological progress and propose adequate strategies for circumventing them.

Financial and staff report

The contributions to ASTEC from the part were lower than expected for 2001. Reasons for this can be attributed to the initiation of a new phase with accompanying recruitment problems and to the general decrease in Swedish economy and the decreasing abilility of industry to carry out and engage in research. The contribution by ASTEC parts during 2001 and budget for 2002 and 2003 are presented in Appendix 5 "Financial report for year 2001 and budget for 2002 and 2003". The cash contributions shown in Appendix 5 is the conribution from VINNOVA and part of Ericssons contribution. The cash flow is shown in Appendix 6. Comparisons of contributions, management costs, man power, cost per man year, cost per publications and staff categories is given in Appendix 3.

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Stappert, F., Ermedahl, A., and Engblom, J. 2001.
Efficient Longest Executable Path Search for Programs with Complex Flows and Pipeline Effects
Technical reports from the Department of Information Technology. ps , pdf , abstract , webpage

Appendix 2

Degrees

PhD-thesis

Fredlund, L.-Å. 2001. A Framework for Reasoning about Erlang Code

Master of Science exams.

Flink, F. 2001. Simuleringsverktyg för kvantifiering och verifiering av distribuerade realtidssystem. Examensarbeten på Datorteknik, Chalmers.

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Nilsson, Magnus 2001. Time Accurate Simulation. UPTEC F 01 074, Masters degree project vol: SEP pages: 1-39.

All theses can be found via ASTEC publication page "http://www.astec.uu.se/publications/".

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Appendix 3

Business ratios for ASTEC 1995 - 2001

ASTEC business ratios are calulated from the costs and activities each year. There is no profit within ASTEC. Contributions from the parts are consumed the same year. The research results are transferred to the participating companies that may profit from them and according to the contracts share the profit with the researchers.

The following tables and figures i summarized here.

The contributions to ASTEC has increased for the first 5 years (1a, b). The increase 1999-2000 is partly due to increased contributions by NUTEK. Their contribution has leveld out on 6 MSEK per year during phase 3 (2001-2003). The first year of Phase 3 has been a year with a drop in industrys ability to support research and a shift in project sturcture with accopmanying reqruitment problems both has contributed to the decerased contributions due to decreased ability to carry out research.

Management costs has increased in absolute values but declined relative to total costs during 1997 -2000 (1a). Year 2001 were calculation of acutal cost instead of schablon cost used which inrease the cost and also the shown academy contribution. Management includes all expences exept direct research.

The cost for each man-year decreased to 55% of its inital value in 1998 and has since then been rather contant (1a).

The amount of work carried out (man years) has increased with about 40% per year during the first 5 years (2a). During year 2001 the amount of work carried out has (as expected) leveld out. During the year has all the amount of all categories diminshed with the largest decrease in industry research staff. Technical/administrative staff has decreased each year (2b).

The publication rate decreased during 2001 compared to year 2000 due to the shift in project structure (3a). It take a while for new projects to obtain results to publish, a similar phenomenom can be seen both 95 and 97-98. The increased cost per publication and time requirement per publication also reflects the start of phases 1, 2 and 3 (1a and 3c). In the early 2002 we can already see an increase in publications (not shown). A interesting shift to journal publication from conference publication has occured during the 2001. This research area has for long been lacking journals to publish in, this reflects the appareance of more jounals in the research field. The major publication type in this field of research is conferences (with referee system), technical reports and workshops(3a,b).

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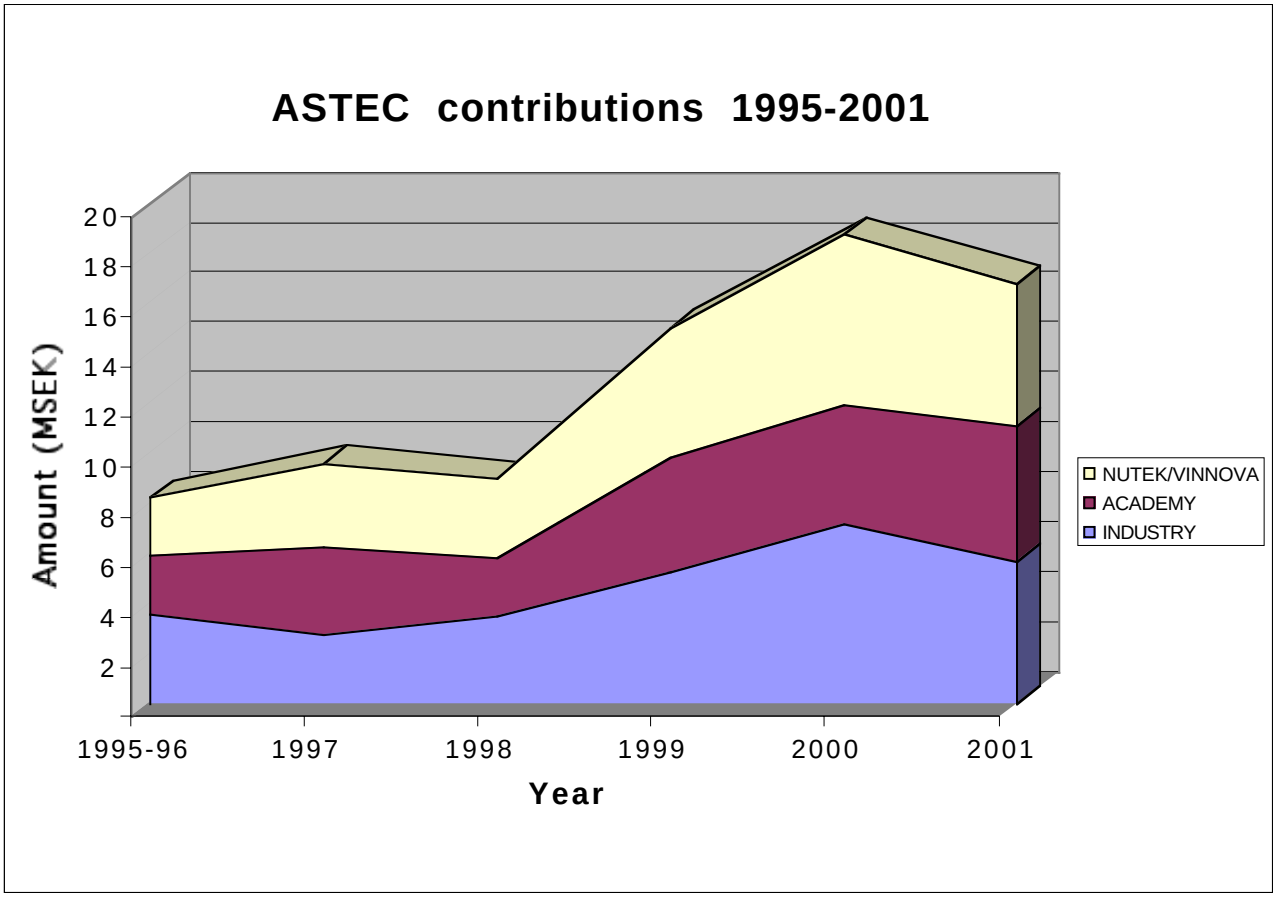
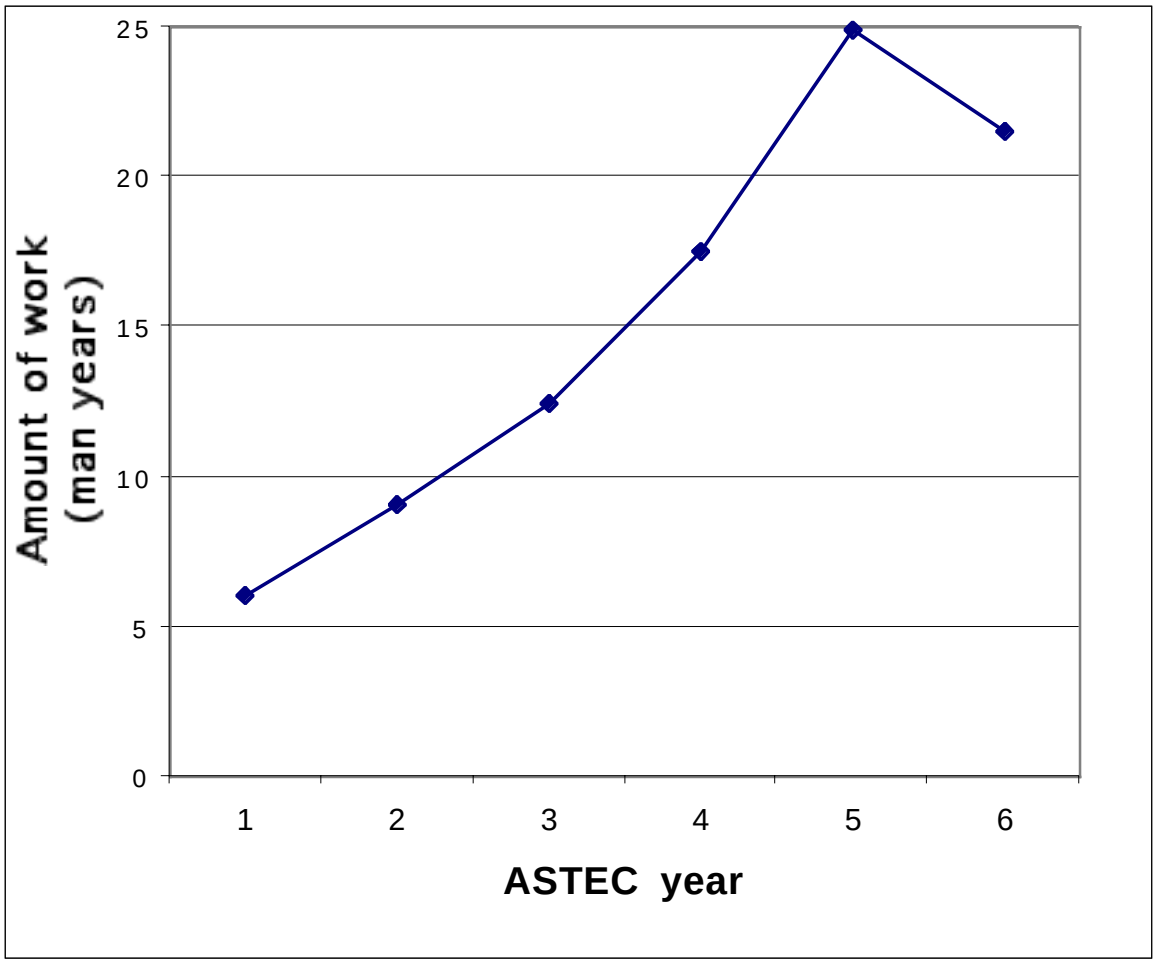
1a) **ASTEC Business Ratios**. The contributions by ASTEC parts, Management, Man power and Publication form the basic data for; the cost per man year (KSEK/man year); the publication cost (KESK/publkication); the effort per publication (man years/publication); the relative management cost (Management/Total).

	Year						
Contributions by	**1995-96**	**1997**	**1998**	**1999**	**2000**	**2001**	**Sum**
INDUSTRY	3568	2778	3520	5293	7219	6117	28495
ACADEMY	2375	3450	2347	4557	4688	5392	22809
NUTEK/VINNOVA	2295	3395	3134	5202	6869	5712	26608
Total (KSEK)	8238	9623	9001	15053	18777	17221	77912
Management (KSEK)	380	818	721	1038	1066	1336	5359
Man power(man years	6,0	9,1	12,5	17,5	25,0	21,5	91,6
Publications (no.)	8	19	12	22	34	28	123
							Mean
KSEK/man year	1371	1054	719	858	753	801	850
KSEK/Publication	1030	506	750	684	552	615	633
Man years/publicatior	0,75	0,48	1,04	0,80	0,73	0,77	0,75
Management/Total	5%	9%	8%	7%	6%	8%	7%

1b) The development of contributions to ASTEC by NUTEK, Academy and Industry.



2a) Development of ASTEC man years.

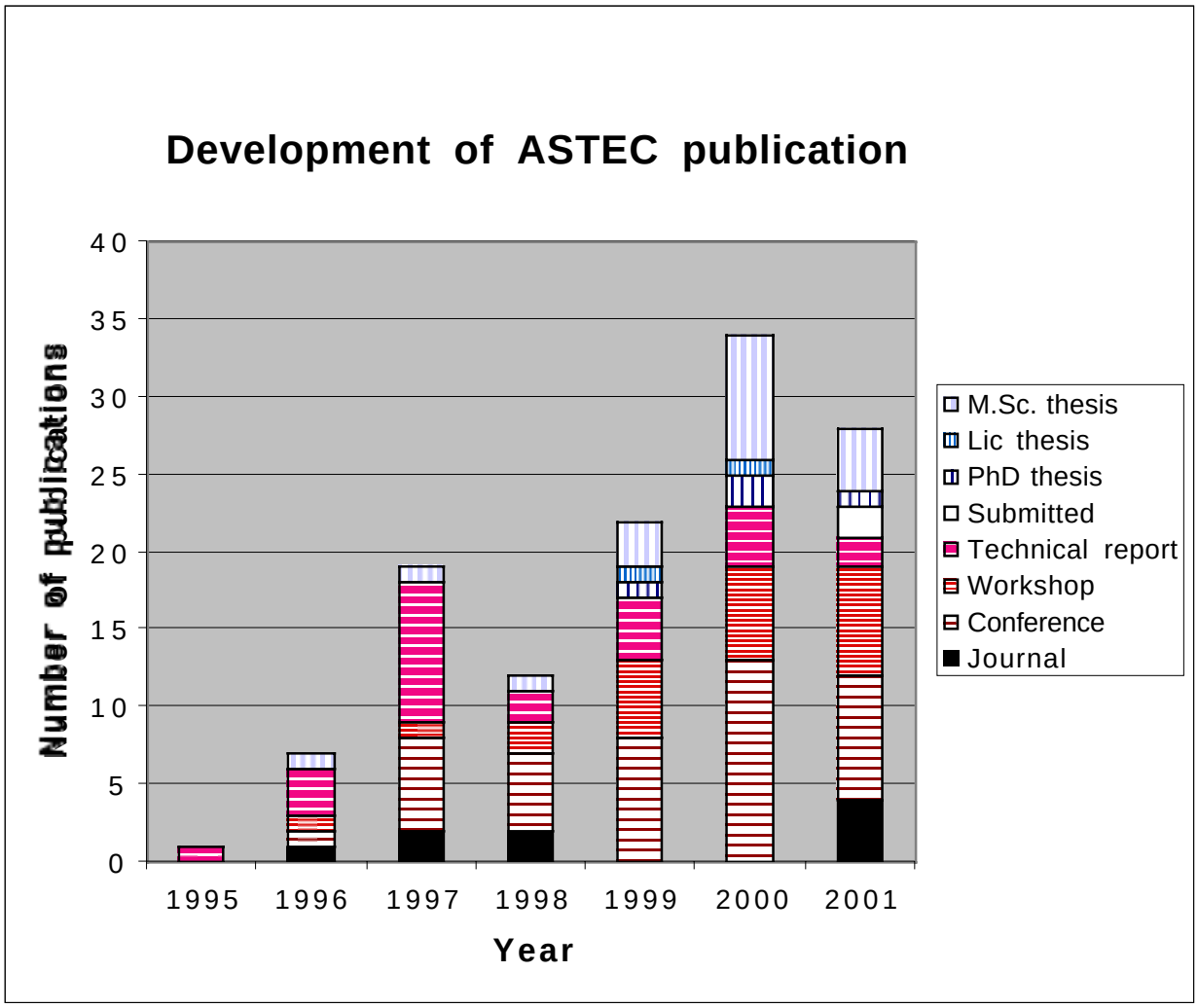


2b) Development of ASTEC staff categories, note the recent increase in Professors, Industry researcher and PhD-students and M.Sc. students.

	Amount each year (man years)					
Category	**1995-1996**	**1997**	**1998**	**1999**	**2000**	**2001**
Professor	0,5	0,3	0,6	0,6	2,1	1,8
Senior researcher	1,2	2,1	2,5	4,1	2,8	2,4
PhD student	3,3	4,1	6,3	7,1	9,0	8,1
Industry researcher	1,0	1,7	2,2	2,1	3,8	1,7
Industry PhD students				2,0	3,0	3,0
Master of Science students				1,0	3,9	3,2
Technical/administrative		1,1	1,0	0,6	0,5	0,4
Total=	6,0	9,1	12,5	17,5	25,0	20,5
Increase each year (man years)	-	3,1	3,4	5,0	7,4	-4,4
Increase each year (%)	-	52%	37%	40%	42%	-18%

Publications and exams

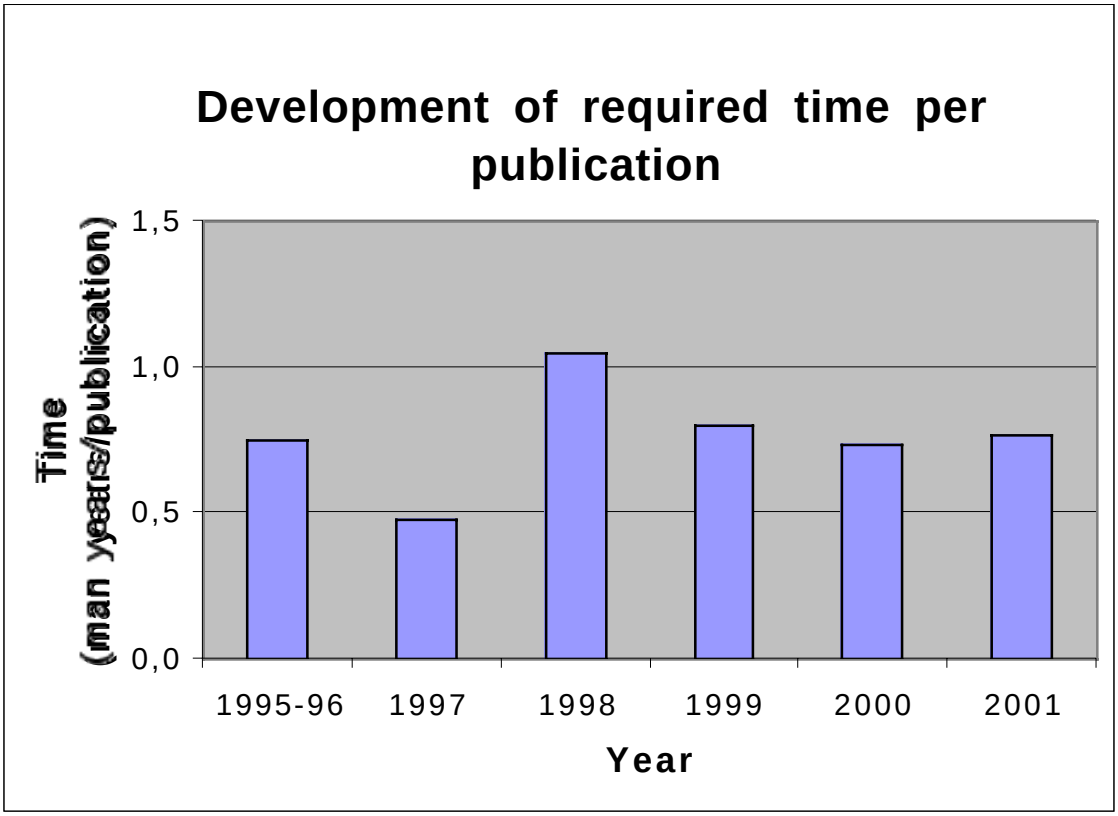
3a) Publication rate, note the increase and the shift from phase 1 to phase 2 1997-1998.



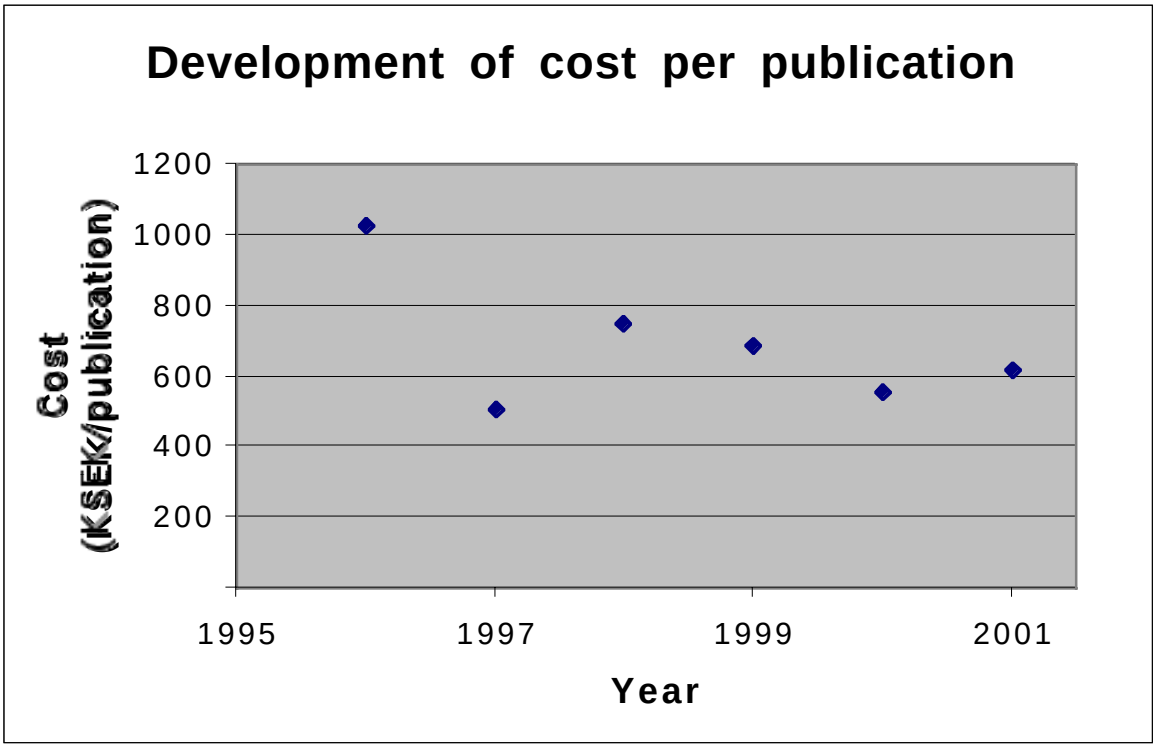
3b) Publication divided into differernt publication categories, note that conference, technical reports, workskop and theses are dominating.

Publications type	Year							
	1995	1996	1997	1998	1999	2000	2001	Sum
Journal	0	1	2	2	0	0	4	9
Conference	0	1	6	5	8	13	8	41
Workshop	0	1	1	2	5	6	7	22
Technical report	1	3	9	2	4	4	2	25
Submitted	0	0	0	0	0	0	2	2
PhD thesis	0	0	0	0	1	2	1	4
Lic thesis	0	0	0	0	1	1	0	2
M.Sc. thesis	0	1	1	1	3	8	4	18
Sum	1	7	19	12	22	34	28	123

3c) Time requirement and cost per ASTEC publication, note the decrease in time per publication as a new phase develops. Phase 1 started 1995 and phase 2 started 1998.



3c) The cost per ASTEC publication, note the decrease in cost per publication over time.



Appendix 4

ASTEC Seminars 2001

http://www.astec.uu.se/Seminars

Dec 11, 2001, Semantics-based models for confidentiality of multi-threaded programs Andrei Sabelfeld, Chalmers University of Technology

Dec 4, Efficient Longest Executable Path Search for Programs with Complex Flows and Pipeline Effects. Andreas Ermedahl, Uppsala University

Nov 29, What is a proof engine? Mats Boman, Prover Technology

Nov 27, Using (Timed) Petri Nets for Verification of Parameterized (Timed) Systems Parosh Abdulla, Uppsala University

Nov 23, Segment Order Preserving and Generational Garbage Collection for Prolog Kostis Sagonas, Uppsala University

Nov 12, Storage Allocation for Embedded Processors. Jan Sjödin and Carl von Platen. Uppsala University and IAR Systems AB

Oct 30,Timed Automata with Asynchronous Processes: Schedulability and Decidability Wang Yi, Tobias Amnell, Elena Fersman, Paul Pettersson ASTEC , Uppsala University

Oct 30, Automatic Code Generation for Timed Automata Tobias Amnell, Elena Fersman, Paul Pettersson, Wang Yi ASTEC , Uppsala University

Sept 18,Time accurate simulation Magnus Nilsson, CC Systems AB

Sept 04, Combining Specification Techniques for Processes, Data and Time Prof. Dr. Ernst-Rüdiger Olderog University of Oldenburg

Sept 04, Adapting Gurvich-Karzanov-Khachiyan's Algorithm for Parity Games: Implementation and Experimentation Emmanuel Beffara, Ecole Normale Superieure de Lyon, France.

Aug 28, Extracting the processes structure of Erlang applications Jan Nyström, Department of Computer Systems, Uppsala University

June 12, First steps towards the formal verification of a distributed Video on Demand server Juanjo Sanchez Penas, University of Corunna, (Galicia, Spain) Place: Ericsson, CSLab, conference room,

June 6, RASCAL -- Timestamp-Based Selective Cache Allocation Martin Karlsson Information Technology, Uppsala Architecture Research Team, Uppsala University.

May 29, K. Rustan M. Leino, ESC/Java and Houdini, Compaq Systems Research Center Palo Alto, U.S.A.

April 10, Paul Pettersson, Uppsala University Guiding and Cost-Optimality in UPPAAL

March 22, Henrik Leerberg, IAR Systems A/S, Denmark. UML Statecharts and IAR visualSTATE

March 20, Henning Makholm, Datalogisk Institut, Dept. of Computer Science, University of Copenhagen Region-based memory management for Prolog

March 13, Lars Albertsson, Computer and Network Architectures Laboratory, Swedish Institute of Computer Science Simulation-Based Debugging and Profiling of Soft Real-Time Applications

March 6, Saddek Bensalem, Uppsala University Incremental Verification by Abstraction

February 27, Jens Knoop, University of Dortmund, Germany Parallel Optimization of Parallel Programs

February 27, Antonin Kucera, Masaryk University Brno Decidability and Complexity Issues for One-Counter Machines

January 30, Lars-åke Fredlund, ASTEC, SICS A formal semantics for a subset of Erlang

January 16, Johnny Burlin, ASTEC, IAR Systems AB Optimizing Stack Frame Layout for Embedded Systems

January 12, 2001, Prof Melvin Fitting, Department of Mathematics and Computer Science, Lehman College, New York. Modal logics between propositional and first-order

Financial report for ASTEC year 2001 and budget for 2002 and 2003

					updated*		see note **		**Phase 3**	
	Budget 2001	**Result 2001**	% of budget	division	**Budget 2002**	division	**Budget 2003**	division	kr	division
ABB Automation Products	112 000	103 000	92%		112 000		112 000		327 000	
Cross Country Systems AB	500 000	150 000	30%		250 000		250 000		650 000	
ENEA OSE Systems AB	280 000	287 230	103%		50 000		250 000		587 230	
Ericsson Utvecklings AB	2 550 000	2 326 080	91%		890 700		890 700		4 107 480	
ESAB	25 000	-	0%		25 000		-		25 000	
I.A.R. Systems AB	2 500 000	2 371 200	95%		1 950 000		1 650 000		5 971 200	
Prover Technology AB	800 000	200 000	25%		500 000		500 000		1 200 000	
Telelogic Sverige AB	500 000	200 000	40%		200 000		200 000		600 000	
Validation AB	675 000	382 500	57%		675 000		675 000		1 732 500	
Virtutech AB	300 000	-	0%		240 000		300 000		540 000	
Volcano Communicaton Technologies AB	150 000	-	0%		100 000		100 000		200 000	
Volvo Teknisk Utveckling AB	150 000	97 000	65%		100 000		150 000		347 000	
New partner(s)							1 720 000		1 720 000	
Industry	8 542 000	6 117 010	72%	36%	5 092 700	31%	6 797 700	37%	18 007 410	34%
Uppsala Universitet inkl MDH	4 262 407	4 125 542	97%		4 473 046		4 473 046			
SICS	1 060 800	307 413	29%		-		-			
MDH		959 030			959 030		959 030			
Akademy	5 323 207	5 391 985	101%	31%	5 432 076	33%	5 432 076	29%	16 256 138	31%
VINNOVA* **	6 000 000	5 711 969	72%	33%	6 080 465	37%	6 207 566	34%	18 000 000	34%
SUM	19 865 207	17 220 964	87%	100%	16 605 241	100%	18 437 342	100%	52 263 548	100%

* Original budget the same contribution each year, the amounts are given in the column "Budget 2001".

** ASTEC managemet budget assumption of contributions for 2003.

*** VINNOVA funding amounts is shown as the year they are consumed. The payment of the contribution is exactly 6 MSEK per year.

ASTEC Cash report

	Result 2001	Budget 2002	Budget 2003
Income	**kr**		
Contribution from VINNOVA/NUTEK	3 000 000	6 000 000	6 000 000
Advance payment	3 717 096	2 335 013	1 299 548
From Ericsson to HiPE project	700 000	600 000	600 000
From ESAB to CODER	-	25 000	
Interest	108 340	80 000	80 000
Sum	**7 525 436**	**9 040 013**	**7 979 548**
Advance payment within projects			
HIPE	378 583	573 000	
SA	527 824	-	
Sum	**906 407**	**573 000**	
Expences		3% increase per year added	
Projects			
CODER	-	-	-
TAS	-	-	-
WCET in Uppsala	855 291	660 712	-
WCET in Västerås (delayed payment 01)	-	1 126 650	588 800
WPO (some of SA advance is included)	758 505	586 379	487 306
HiPE (including advance payment)	1 561 000	2 384 635	2 456 174
ErlVer	307 413	-	-
SA (including advance payment)	134 266	-	-
SAAPP	-	500 274	515 283
Automated testing	141 667	468 650	482 710
SMC (delayed payment for 2000 & 2001)	200 000	813 825	517 189
Software Synthesis	655 000	705 550	726 717
Analysing ERLANG/OTP systems	212 500	380 242	-
Summa projekt	**4 825 642**	**7 626 917**	**5 774 177**
Administration, kick off, pr, etc			
Tax (Högskolemoms 8% on Ericsson to HiPE)	56000	48000	48000
Administration	**606 327**	**638 548**	**650 000**
Equipment	35 861		
Calculated advance payment 200x-12-31	2 335 013	1 299 548	**1 507 372**
			Left for disposal during phase 3

Längre driftstid med energisnåla datorprogram

Konstruktion av datorprogram för minimal energiförbrukning är målet för forskning som bedrivs vid Uppsala universitet. Där har forskare utvecklat en metod som förklarar hur mycket energi en processor förbrukar beroende på hur dess datorprogram är skrivet.

Exempel på apparater med batteridrivna datorsystem

Hela samhället har under de senaste decennierna blivit all mer beroende av datorer. Detta gäller inte bara de gråa lådor som står på våra skrivbord utan även de ”osynliga” datorsystem som finns i alla de saker som vi använder till vardags, från bilar och flygplan till mikrovågsugnar, mobiltelefoner och leksaker. Många av dessa inbyggda datorsystem har batterier som huvudsaklig strömkälla och är därför beroende av energisnål design för att uppnå lång driftstid. För att maximera tiden mellan byten och/eller uppladdningar av batterier har de senaste åren en intensiv forskning och utveckling skett på energisnål batteri- och hårdvarudesign. På IT-institutionen vid Uppsala universitet går man steget längre och forskar i hur själva programmet som datorn kör skall konstrueras för att minska energikonsumtionen ytterligare.

En modern dator är ett komplicerat system bestående av många olika komponenter som alla bidrar i varierande grad till den totala energiförbrukningen. Program skrivna på olika sätt använder olika delar av datorn olika mycket och kan därför ge varierande energiförbrukning. Detta öppnar för möjligheten att skriva program för låg energiförbrukning. Men precis som en bilförare vill kunna köra en bil utan att behöva hålla reda på hur bilens motor och elektriska system egentligen fungerar, så vill en programmerare kunna skriva datorprogram utan att ha en alltför detaljerad kunskap om datorns inre uppbyggnad och funktion.

Generell analysmetod

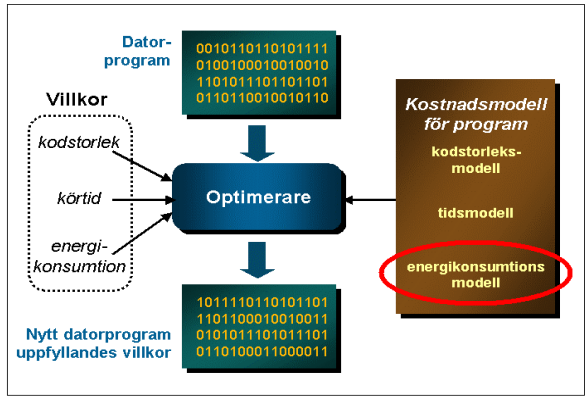
Doktoranden Andreas Ermedahl vid Uppsala universitet har tillsammans med forskare vid Seoul National University i Korea tagit fram en metod för att förklara varför olika datorprogram förbrukar olika mycket energi. En processor är själva hjärnan av en dator och kan sägas vara den enhet som organiserar själva arbetet som datorn utför. En dator består även av ett antal andra enheter som samverkar med processorn för att kunna utföra de önskade uppgifterna. Den utvecklade metoden använder mätningar på en processor och statistiska analysmetoder för att ta fram en enkel och användbar modell för energiförbrukningen.

– Metoden har hittills använts för att ta fram en modell för energikonsumtionen av en ARM7-processor, men då analysmetoden inte kräver någon detaljerad kunskap av processorns inre uppbyggnad är den lätt att använda även på andra processorer. Något som är viktigt med tanke på den stora variation av hårdvara som används i dagens inbyggda system, säger Andreas Ermedahl.

Optimering för energi

Ett datorprogram består av en mängd instruktioner som tillsammans utgör en beskrivning på hur datorn skall lösa en uppgift. Exempel på sådana instruktioner är att addera två tal eller hoppa till en viss instruktion i programmet. Ofta är det, genom att använda olika instruktioner, möjligt att skriva flera, mer eller mindre lika, program för att utföra en viss uppgift. När man optimerar ett datorprogram för en viss egenskap skriver man om programmet så det fortfarande utför sin ursprungliga uppgift men samtidigt försöker uppnå den önskade egenskapen.

Med den nya analysmetoden införs en ny dimension av möjliga optimeringar av datorprogram. Hittills, för att kunna uppnå hög prestanda och funktionalitet med billig hårdvara, har forskare och industrin fokuserat på optimeringsmetoder för att minimera storleken på och/eller körtiden av program. Med hjälp av en korrekt energiförbrukningsmodell blir det även möjligt att optimera datorprogram för minimal energiförbrukning. Något av stor betydelse för den industri som utvecklar inbyggda system och i slutändan även för konsumenten som får bättre produkter med längre driftstider.



Med en korrekt energikonsumtionsmodell kan man optimera program för minimal energiförbrukning

Avancerad mätutrustning

För att kunna skapa en korrekt energiförbrukningsmodell användes avancerad mätutrustning utvecklad av en koreansk forskargrupp. En modern processor, som den analyserade ARM7-processorn, utför 100 000-tals instruktioner per sekund. Den utvecklade mätutrustningen gör det möjligt att mäta energin förbrukad av processorn på en detaljnivå av varje enskilt utförd instruktion. Förutom enstaka instruktioners påverkan lyckades man, med hjälp av statiska analysmetoder, isolera andra faktorer som påverkade energikonsumtionen ytterligare, t.ex. på vilken plats i programmet en instruktion befinner sig, värdena av de tal som adderas av en instruktion, eller vilka instruktioner som körs efter varandra. Alla dessa faktorer formade tillsammans en modell för att förutsäga processorns totala energikonsumtion.

Hittills har inte hela instruktionsuppsättningen för ARM7-processorn analyserats. För de instruktioner som analyserats lyckas dock den härledda modellen förutsäga den förbrukade energin med ett genomsnittligt fel på 2.5 procent. I framtida arbete ligger, förutom att undersöka kvarvarande instruktioner, att analysera andra enheter i datorn än just processorn. – Det är först med en modell som tar hänsyn till energiförbrukningen hos alla enheter i datorn som de riktigt stora energivinsterna kan göras, avslutar Andreas Ermedahl.

Samarbete över nationsgränser

Arbetet för att skapa en korrekt modell för en datorns energiförbrukning är ett pågående forskningssamarbete mellan Uppsala Universitet och Seoul National University i Korea. Hittills uppnådda resultat har presenterats för expertis vid internationellt ansedda konferenser.

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