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ASTEC
Advanced Software Technology

ASTEC

Advanced Software Technology

This document is the

Report for year 7

(2002: the second year in phase 3)

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Up-to-date information about current activities can be found on the
WWW page http://www.astec.uu.se/

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Summary

The main results of ASTEC during year 7.

1. The foundation to increase the number of companies participating in ASTEC from 12 to 14 has been laid in 2002.
2. During 2002, in addition to numerous publications, 2 Ph.D. theses, and 6 M.Sc. theses have been completed.
3. Information dissemination efforts have been maintained on a high level in the form of seminars and presentations of research results at conferences.
4. Several graduate courses and seminars have been conducted.
5. One project has been concluded in 2002 and a new one has been initiated.
6. The HIPE (High Performance Erlang) compiler has been incorporated as an integrated component as a default component into the distribution of the Erlang/OTP system from Ericsson.
7. The general decline in the IT area is reflected in ASTEC business ratios.
8. The direct and indirect involvement of ASTEC into research under the auspices of the EU is increasing. ASTEC has been instrumental in developing a basis for participation in the ARTIST European Research Network.

Sammanfattning

De viktigaste resultaten av ASTEC under år 7.

1. Under 2002 har en grund lagts för att utöka antalet näringslivsintressenter från 12 till 14.
2. Under 2002 har ett flertal publikationer, två doktorsdisputationer och sex examensarbeten presenterats.
3. Informationsspridningen genom seminarieserier har fortsatt på en hög nivå liksom presentationerna på konferenser.
4. Flera doktorandkurser och seminarier har hållits.
5. Ett forsknngsprojekt har avslutats och ett nytt har påbörjats under 2002.
6. HiPE kompilatorn har inlämmats som en standardkomponent i Open Source Erlang/OTP.
7. Den övergripande nedgången inom IT sektorn avspeglas även i ASTEC:s nyckeltal.
8. Engagemanget i EU-projekt ökar kontinuerligt. ASTEC forskare är delaktiga i det Europeiska forskarnätverket ARTIST.

Contents

Introduction

ASTEC (Advanced Software Technology) is a competence centre that focuses on Advanced Tools and Techniques for Software Development. Development of software systems, such as large telecommunication, transportation and process control systems, accounts for a significant part of the costs in the construction of a number of important products of the Swedish industry. It is thus of vital interest to be able to produce better software at lower costs. One of the means to achieve this is to improve the tools and techniques used for software development. ASTEC's vision is that, wherever possible, software should be developed using high-level specification and programming languages, supported by powerful automated tools that assist in specification, analysis, validation, simulation, and compilation. The purpose of ASTEC is to conduct pre-competitive and industrially applicable research that contributes to this vision, to build up and offer a concentrated research environment in the software technology area, and to be a forum for contacts and exchange of ideas between academia and industry.

ASTEC has been formed as a consortium of academic partners with strong research programs in different areas of software technologies and of companies that either have a substantial software production or produce tools for software development. During the first two three-year phases of ASTEC, the focus of ASTEC was to connect academia with industry by conducting projects where techniques from academia were applied to problems in industry. This effort created a network of contacts between academia and industry. During its third three-year phase, ASTEC

has developed into a focussed and distinct research unit, having a broad contact area with a number of companies. It is a natural forum for collaboration, discussions, and new contacts in the software technology area within Sweden.

Partners

ASTEC has been formed as a consortium of the following academic and industrial partners during phase 3.

- Research groups at *Uppsala University*, *Mälardalen University*, and SICS working mainly on formal methods, functional, logic and constraint programming, compilation, and on embedded, distributed, and real-time systems, together with
- companies with a substantial software production and thus a large interest in software development. These include companies like: *ABB Automation Products AB, Cross Country Systems AB, Ericsson Utvecklings AB, ESAB Welding Equipment AB, Validation AB, and Volvo Teknisk Utveckling AB,* and
- companies that produce tools for software development: *ENEA Ose Systems AB, IAR Systems AB*, *Prover Technology AB*, *Telelogic Sverige AB*, *Virtutech AB*, and *Volcano Communication Technologies AB*.

General Observations

In 2002 and more generally during the transition from Phase 2 to Phase 3 of ASTEC, the following general points are notable.

- Various projects have matured, they have delivered tools and results to their industrial partners that are being used and have an impact in their corresponding domains.
- There has been a shift in technical focus of several projects, especially within the Validation and Verification areas of ASTEC. Compared to Phase 2, in Phase 3 there is less emphasis on formal verification, whereas more attention is paid to other verification techniques, such as testing, program analysis, and simulation. In addition, new activities on code generation and scheduling have started.
- The level of activities during 2002 is about the same as that of 2001 but is however lower than that of 2000. This is due to the problems faced by the IT/SW industry that is responsible for difficulties in obtaining a sufficient level of matching funds from industry during 2002.
- Results of ASTEC's work have been disseminated for industrial usage. Notable among these are
  - the **HiPE** compiler, which has been incorporated into the open source release of Erlang/OTP since September 2001 and is available by default in the Erlang/OTP release of October 2002,
  - the **TIMES** schedulability analysis tool which is downloadable from the net,
  - work from the SMC project that has been incorporated into tools from **Prover,** and
  - an online test oracle generator was ported to the Simulink environment and delivered to **Volvo**.

General Figures

During 2002, numerous publications in various well-established international conferences and journals, including 2 Ph.D. theses, and 6 M.Sc. theses have been produced (see Appendix 1 and 6). Within the ASTEC seminar series, a total of 21 seminars were conducted (Appendix 2). A comparison with previous years is given in Appendix 3.

Research Activities

Concluded Projects

Several projects have been concluded at or since the beginning of phase 3.

- The Project **Erlang Verification**, which developed a tool for formal verification of Erlang programs, has been concluded as of summer 2001, by a delivery and demonstration at Ericsson, and by the completion of Lars-åke Fredlund's Ph.D. thesis (September 2001).
- The Project **Static Analysis** has been concluded by a seminar, and by incorporation of results into graduate seminars given during 2001.
- The Project **Auto** has been concluded at the end of Phase 2. The last result is a major case study, in which a car locking system has been modelled and analysed using the UPPAAL tool. Mecel AB has left the ASTEC consortium at the end of Phase 2.
- The Project **BUS**, in which an industrial bus protocol has been modelled and analysed using UPPAAL, has been concluded with an evaluation by ABB. The insights from the BUS project will guide future projects that aim at investigating how to use formal verification technology in industrial software development.

In general, the projects on formal verification have exhibited possibilities and bottlenecks for the application of formal verification within industrial software development. Guided by insights from these projects, new ASTEC activities have started, as described in the next paragraph.

New Projects

Guided by the experiences of previous projects, and by comments made in the evaluation, new projects have been initiated, especially within the area of Verification and Validation.

- The project **Erlang Analysis** (2001-02) developed techniques and a tool for extracting the process structure of Erlang applications from source code. In the Erlang/OTP system there are libraries that can be used to create redundancy and fault-tolerant behaviour in Erlang applications. The developed tool extracts the process structure and analyses it in order to detect potential problems in recovering from failures. The project has concluded at the end of 2002. Jan Nyström is currently writing a Ph.D. thesis on the topic (plan is to defend it in the fall of 2003).
- The project **Software Synthesis** has as it's goal to develop a tool suite, called **TIMES**, for schedulability analysis using timed automata technology, and synthesis of real time software with predictable timing behaviours. In scheduling theory, off-line schedulability tests usually assume that real time tasks are periodic. The assumption of complete knowledge on task uniform arrival times may cause unacceptable resource requirements due to the pessimism in the analysis. **TIMES** uses timed automata to describe task arrival patterns, which yields a unified task model expressive enough to describe concurrency,

synchronization, and real time tasks that may be (non-)periodic and (non-)preemptive. The analysis can handle combinations of timing, precedence and resource constraints. Since its first presentation at TACAS'02, the central algorithm of **TIMES** has been improved greatly due to a recent result [TACAS'03] showing that the schedulability analysis problem for fixed priority scheduling can be done using two clock variables. Due to this result, now **TIMES** can check the schedulability for tasks with general arrival patterns and its efficiency is comparable with classic rate-monotonic analysis, which is only applicable for periodic tasks.

- The purpose of the **Testing** project is to develop tools for generating test sequences for telecommunication protocols and services, which are defined as extended state machines. Within the project, a new activity has started in collaboration with Mobile Arts (a new ASTEC industrial partner). This activity consists of the following sub-activities:
  - A definition of an Erlang format for extended state machines
  - A tool for generation of exhaustive test sequences from definitions of state machines. The test sequences exhaustively test the functional behaviour of one instance of a protocol/service. Under certain conditions, the test execution machinery may be distributed over several nodes (if the protocol under test communicates with several different entities) that need very limited interaction during the test execution.
  - During summer 2003, a first tool will be developed together with a scientific report.
  - Future plans include generation of test with a variety of partial coverage criteria, test generation for testing the interaction between many concurrent instances of a protocol, and to establish a connection with model-checking tools.
- The project **Simulator-Aided Analysis of Parallel Processes (SAAPP)**, in collaboration between UU and Virtutech AB, is aiming to develop techniques for simulation of parallel programs in order to detect possible concurrency problems. The project is based on the SIMICS simulator for multiprocessor systems. Due to difficulties in recruitment during 2001, the actual starting date of the project was April 2002.
- The purpose of the project **TAS: Time-Accurate Simulation of Distributed Embedded Real-Time Systems** is to add mechanisms to enable simulations of Distributed Embedded Systems to be performed in actual real-time on a powerful workstation or PC. The approach is to analyze actual execution times of code segments, and use timers to control the scheduling of processes on the workstation.

Other significant activities during 2002 were:

- In connection with the project Software Synthesis, M.Sc. projects in collaboration between UU and ABB, investigated how to use formal verification technology in industrial software development.
- In connection with the project on Erlang Verification, Ericsson UA developed tools for generating models from Erlang programs that are subject to model checking. In a recently concluded project, techniques for visualizing and analysing traces generated during execution of Erlang programs have been developed.
- The project on testing has been expanded by a Ph.D. student, and by associating one more senior researcher. In the beginning of 2002, a seminar series in the area has been conducted.

Change in Project Focus

The project **Symbolic Model Checking (SMC)**, which develops techniques for using satisfiability checking in system verification, has previously focussed on using satisfiability checking as a tool in model checking of hardware designs. Since the beginning of phase 3 of ASTEC, the focus has shifted to analysis of fault trees, and how satisfiability checking can be used for this problem.

Industrial Exploitation

ASTEC is on its way to make research results industrially exploitable.

- The major goal of the **HiPE (High Performance Erlang)** project has been the full incorporation and integration of the HiPE compiler in the Open Source Erlang implementation from Ericsson. This goal is now fully accomplished. It has been achieved in three steps: First, HiPE was ported to the latest Erlang/OTP implementation (Release 7B-1). This step was completed in February 2001. Since then, a much closer co-operation between the HiPE team and the Erlang/OTP team from Ericsson was established through very frequent exchange of code snapshots. This has resulted in incorporating HiPE into the main branch of the Erlang development and HiPE was finally released together with the pre-release and the final release of Erlang/OTP R8 (October 2001). Since experience from using HiPE in the Erlang user community was positive, a decision was made to have HiPE as a fully integrated and supported component in Erlang/OTP R9B (released in October 2002). See also Erlang/OTP's homepage.
- A **back-end of HiPE for the Intel x86 architecture**, which is an important development platform these days, was designed and developed. A lot of effort was put so that this port reached the level of maturity and robustness that is expected from an industrial-strength Erlang compiler. Results show that the resulting system, HiPE/x86, is significantly faster than the Ericsson implementation of Erlang, and achieves speedups comparable to and sometimes better than those of the more mature HiPE/SPARC compiler. This compiler is also included in Erlang/OTP Release 8B, and is used by the Erlang community. This particular work has resulted in a publication in a major conference of the area (FLOPS'02). Some remaining x86-specific compiler improvements are planned during the first half of 2003.
- The **TIMES** tool, described in detail in a paragraph above, can now be freely downloaded from **www.timestool.com** for applications in research and education.
- The **Erlang Analysis** project has produced a prototype implementation to analyze supervision trees of Erlang applications. The tool has been able to analyze a significant number of existing OTP applications (however, it did not uncover any really surprising results). It is unclear how the implementation will be used/developed in the future.
- The **WCET** project has conducted several case studies, with the aim of evaluating the usefulness of WCET technology for industrial applications. There are currently discussions to develop a commercial WCET tool, in collaboration between IAR Systems AB, and a small Finnish company.

Collaboration

Within ASTEC and its partners

- The projects **WPO** (Whole Program Analysis), **WCET** (Worst Case Execution Time) and **TAS** (Time Accurate Simulation) are closely collaborating within the **CODER** cluster, which engages a total of 4 companies. The collaboration concerns infrastructure for a C compiler, joint organization of graduate courses, and joint project meetings.
- A very close collaboration between members of the **HiPE** project and the **Erlang/OTP** development team at Ericsson Utveklings AB has been established.

National Collaboration

The national research programme ARTES which supports research and promotes graduate education, hosted at Uppsala University and funded by SSF (The Swedish Foundation for Strategic Research) with a budget of 88MSEK during 1998-2002, was initiated in 1998 with the support and involvement of several ASTEC researchers. Currently, Prof. Hans Hansson is program director. Profs Hansson together with Parosh Abdulla and Wang Yi conduct projects funded by ARTES. There is a close coordination between ASTEC and ARTES work: the two bodies share Roland Grönroos as administrator, and several ASTEC projects are closely related to ARTES projects.

International Collaboration

- UU and MdH have engaged in the preparation for the 6th Framework Programme, by participating in the **ARTIST** Initiative. **ARTIST** (Advanced Real Time Systems in IST) brings together around 20 strong research groups in Europe in the area of Advanced Real Time Systems. The objective of **ARTIST** is to
  - Improve awareness of academics and industry in the area, especially about existing innovative results and technologies, standards and regulations.
  - Define innovative and relevant work directions, identify obstacles to scientific and technological progress and propose adequate strategies for circumventing them.

  Uppsala has coordinated one of these efforts, viz. on "*component-based development for embedded systems*".
- The **SMC** group and **Prover** have a close collaboration and participation within the EU project **ESACS** (Enhanced Safety Assessment for Complex Systems).
- The **Testing** project is communicating with the EU funded RT network **GAMES**, which concerns basic research on testing theory, trying to apply results from game theory.

Graduate Education

Members of ASTEC have been organizing the following graduate seminars/courses

- A seminar series on testing, organized by Prof. Bengt Jonsson and Paul Pettersson, has been given in two instances: one in Spring 2002 and one in Autumn 2002.

- A national graduate course in computer science (CUGS) on real-time and embedded systems as well as a course on the use of formal methods for real-time systems has been conducted by Prof. Wang Yi.
- A graduate level programming language implementation seminar focussing on just-in-time compilation and memory management of high-level languages has been conducted by Konstantinos Sagonas.
- A graduate level programming language implementation seminar focussing on region and escape analysis, and certifying compilation has been organized by K. Sagonas.

Dissemination

- Several implementation aspects of the **HiPE** system have been presented at various universities in Europe (e.g. at the Technical University of Madrid, at DIKU in Denmark, and at Universities in the Czech Republic) and in Japan.

- Several demos of aspects of the **TIMES** tool have been given at conferences (e.g. at TACAS) and universities (e.g , at United Nations University in Macau and the National University of Singapore).

- Presentation of the **testing** work at the **GAMES** project meeting, Edinburgh, Sept 2002.

- Articles in Elektroniktidningen about **WCET** and an article in Dagens Nyheter (DN) on Jakob Engblom's Ph.D. thesis.

Strategies for Long Term Development

The direct and indirect involvement of ASTEC into research under the auspices of the EU is increasing. ASTEC has been instrumental in developing a basis for participation in European Research Networks.

- The **WOODDES** (Workbench for Object Oriented Design and Development of Embedded Systems) project is devoted to development technology for embedded systems in automotive and telecommunication industry within the framework of UML. The project has 6 industrial partners, representing European automotive industry, telecommunication and tools developers and 2 academic partners: Oldenburg University, Germany and Uppsala University.
- The European **VERIFICARD** project will study security aspects of the JavaCard programming platform for Smartcards, by means of software verification techniques. A contribution will be to adapt our work on compositional proof techniques developed within ASTEC.
- The **ADVANCE** project "Advanced Validation for Telecommunication Protocols", will develop tools that extend the power of formal analysis. Its partners include Uppsala and Ericsson. Our participation in all these projects builds directly on ASTEC work.

Financial and staff report

The contributions to ASTEC from its industry partners were lower than expected for 2002. Reasons for this can be attributed to the general problems that the Swedish IT/SW business (and its telecommunication sector in particular) is currently facing and the decreasing ability of industry to carry out and engage in research. The contribution by ASTEC parts during 2001 and budget for 2002 and 2003 are presented in Appendix 4 "Financial report for years 2001 and 2002 and budget for 2003". The cash contributions shown in Appendix 4 are the contribution from VINNOVA and part of Ericsson's contribution. The cash flow is shown in Appendix 5. Comparisons of contributions, management costs, manpower, cost per man-year, cost per publications and staff categories are given in Appendix 3.

ASTEC

Appendix 1

Degrees Awarded

Ph.D. Theses

1. Erik Stenman. **Efficient Implementation of Concurrent Programming Languages**.
   Uppsala Dissertations from the Faculty of Science and Technology No. 43.
   Uppsala University, November 2002.
2. Jakob Engblom. **Processor Pipelines and Static Worst-Case Execution Time Analysis**.
   Uppsala Dissertations from the Faculty of Science and Technology No. 36.
   Uppsala University, April 2002.

Master of Science Theses

1. Per Gustafsson. **Native Code Compilation of Erlang's Bit Syntax.** Uppsala Tekniska Högskola Master Thesis, UPTEC F 02 076, Uppsala University, October 2002.
2. Tobias Lindahl. **Compilation of Floating Point Arithmetic in the High Performance Erlang Compiler.** Uppsala Tekniska Högskola Master Thesis, UPTEC F 02 07, Uppsala University, October 2002.
3. Martin Karlsson. **Memory Characterization of the ECperf Benchmark.** Uppsala Master Thesis in Computer Systems, Uppsala University, May 2002.
4. Jonas Boustedt. **Inferring Structure of WWW Services for Testing.** Uppsala Master Theses in Computer Systems, Uppsala University, April 2002.
5. Jesper Wilhelmsson. **Exploring Alternative Memory Architectures for Erlang: Implementation and Performance Evaluation**. Uppsala Master Thesis in Computing Science 212, Uppsala University, April 2002.
6. Martin Karlsson. **Worst Case Execution Time Analysis, Case Study on Interrupt Latency for the OSE Real-Time Operating System.** KTH Master Thesis in Electrical Engineering, Stockholm, 18 March 2002.

All theses can be accessed via ASTEC publication page "http://www.astec.uu.se/publications/".

Appendix 2

ASTEC Seminars 2002

http://www.astec.uu.se/Seminars

Nov 14, ASTEC, Half-Day-Seminar
Results from the Erlang/HiPE cluster.

Nov 1, Efficient Implementation of Concurrent Programming Languages.
Erik Stenman, Uppsala University

Oct 21, Compilation of Floating Point Arithmetic in the High Performance Erlang Compiler
Tobias Lindahl, Uppsala University

Oct 1, Expressive Power of Temporal Logics
Alexander Rabinovich, Tel Aviv University, Israel

Oct 2, Native code compilation of Erlang's bit syntax
Per Gustafsson, Uppsala University

Sept 23, On the Complexity of Bisimulation Equivalence for Pushdown Automata
Richard Mayr, University of Freiburg, Germany

Sept 17, A logic of probability with decidable model-checking
Alexander Rabinovich, Tel-Aviv University

Sept 3, Algorithmic Analysis of Polygonal Hybrid Systems
Gerardo Schneider

June 5, Towards Automatic Synthesis of Statistical Data Analysis Programs
Bernd Fischer, Automated Software Engineering Group USRA/RIACS, NASA Ames Research Center, California, USA

June 6, Model Checking Birth and Death
Joost-Pieter Katoen, University of Twente, The Netherlands

May 16, Memory Characterization of the ECperf Benchmark
Martin Karlsson, Uppsala University

May 16, RH Lock: A Scalable Hierarchical Spin Lock
Zoran Radovic, Uppsala University

May 14, Timing analysis of an SDL subset in Uppaal.
Anders Hessel, Department of Information Technology, Uppsala University

May 13, Semantic Web and Formal Specifications
DONG, Jin Song, School of Computing, National University of Singapore

April 8, A Process-Algebra-Like Framework for Modelling Hybrid Systems
Michael Baldamus, University of Karlsruhe, Germany

April 2, Exploring Alternative Memory Architectures for Erlang: Implementation and Performance Evaluation
Jesper Wilhelmsson, Uppsala University

March 26, Automated analysis of dynamic web services
Jonas Boustedt, Högskolan i Gävle

March 19, Worst Case Execution Time Analysis, Case Study on Interrupt Latency for the OSE Real-Time Operating System
Martin Carlsson, KTH

March 19, Optimized Instruction Set Simulator Model
Tomas Östlund, Uppsala University

Jan 15, The design and implementation of a soft-typing system for Erlang
Sven-Olof Nyström, Uppsala University

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Appendix 3

Business ratio's for ASTEC 1995 - 2002

ASTEC business ratios are calculated from the costs and activities each year. There is no profit within ASTEC. Contributions from the parts are consumed the same year. The research results are transferred to the participating companies that may profit from them and according to the contracts share the profit with the researchers.

The following tables and figures are summarised here.

The contributions to ASTEC has increased for the first 5 years (Fig 1a, b). The increase during 1999-2000 is partly due to increased contributions by NUTEK. Their contribution has levelled out on 6 MSEK per year during phase 3 (2001-2003). During year 2001 industry's ability to support research has decreased. At the same time a shift in project structure with accompanying recruitment problems caused decreased ability to carry out research. During 2002 the total contributions were recovered. This was achieved by increased contributions from academia. The continued poor trading conditions for industry were probably the cause of the slight decrease in their contributions during 2002.

Management costs has increased in absolute values but declined relative to total costs during 1997 -1999 (Fig 1a) and thereafter stabilised on about 7%. Management includes all expenses except direct research. About 60% of this cost is covered by academy.

The cost for each man-year decreased during the first 3 years to 55% of its initial value. The last years an increase has occurred (Fig 1a). This can be partly be explained by fewer Master of Science students the last year (Fig 2b).

The amount of work carried out per year increased with about 40% per year during the first 5 years (Fig 2a). Since then the amount of work has levelled out. During 2002 ASTEC research funding partly shifted from researchers to PhD-students. A larger amount of the work carried out by researchers was made with other funding from Academia. The number of industrial PhD students decreased partly due to a dissertation followed by recruitment to industry (Fig 2b).Technical/administrative staff has decreased each year (Fig 2b).

The publication rate increased during 2002 compared to year 2001 due to the shift in project structure (Fig 3a). It takes a while for new projects to obtain publishable results, a similar phenomenon can be seen both 96 and 98-99. The increased cost per publication and time requirement per publication also reflects the start of phases 1, 2 and 3 (Figs 1a and 3c). An interesting shift to journal publication from conference publication has occurred during the 2001. The major publication type in this field of research is conferences (with referee system), technical reports and workshops(Figs 3a,b). There is a trend to decreased cost per publication over time.

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1a) ASTEC Business Ratios. The contributions by ASTEC parts, Management, Man power and Publication form the basic data for: the cost per man year (KSEK/man year); the publication cost (KSEK/publication); the effort per publication (man years/publication); the relative management cost (Management/Total).

Contributions by	1995-96	1997	1998	1999	2000	2001	2002	Sum
INDUSTRY	3568	2778	3520	5293	7219	6117	5659*	34154
ACADEMY	2375	3450	2347	4557	4688	5392	6159	28969
NUTEK/VINNOVA	2295	3395	3134	5202	6869	5712	6672	33280
Total (KSEK)	8238	9623	9001	15053	18777	17221	18491	96403
Management (KSEK)	380	818	721	1038	1066	1336	1293	6651
Man power(man years	6,0	9,1	12,5	17,5	25,0	21,5	20,7	112,3
Publications (no.)	8	19	12	22	34	28	33	156
								Mean
KSEK/man year	1371	1054	719	858	753	801	894	858
KSEK/Publication	1030	506	750	684	552	615	560	618
Man years/publicatior	0,75	0,48	1,04	0,80	0,73	0,77	0,63	0,72
Management/Total	5%	9%	8%	7%	6%	8%	7%	7%

*) At the time of writing is there an uncertainty whether one industry contribution of 1.8 MSEK for year 2002 can be counted in. It is included in all tables.

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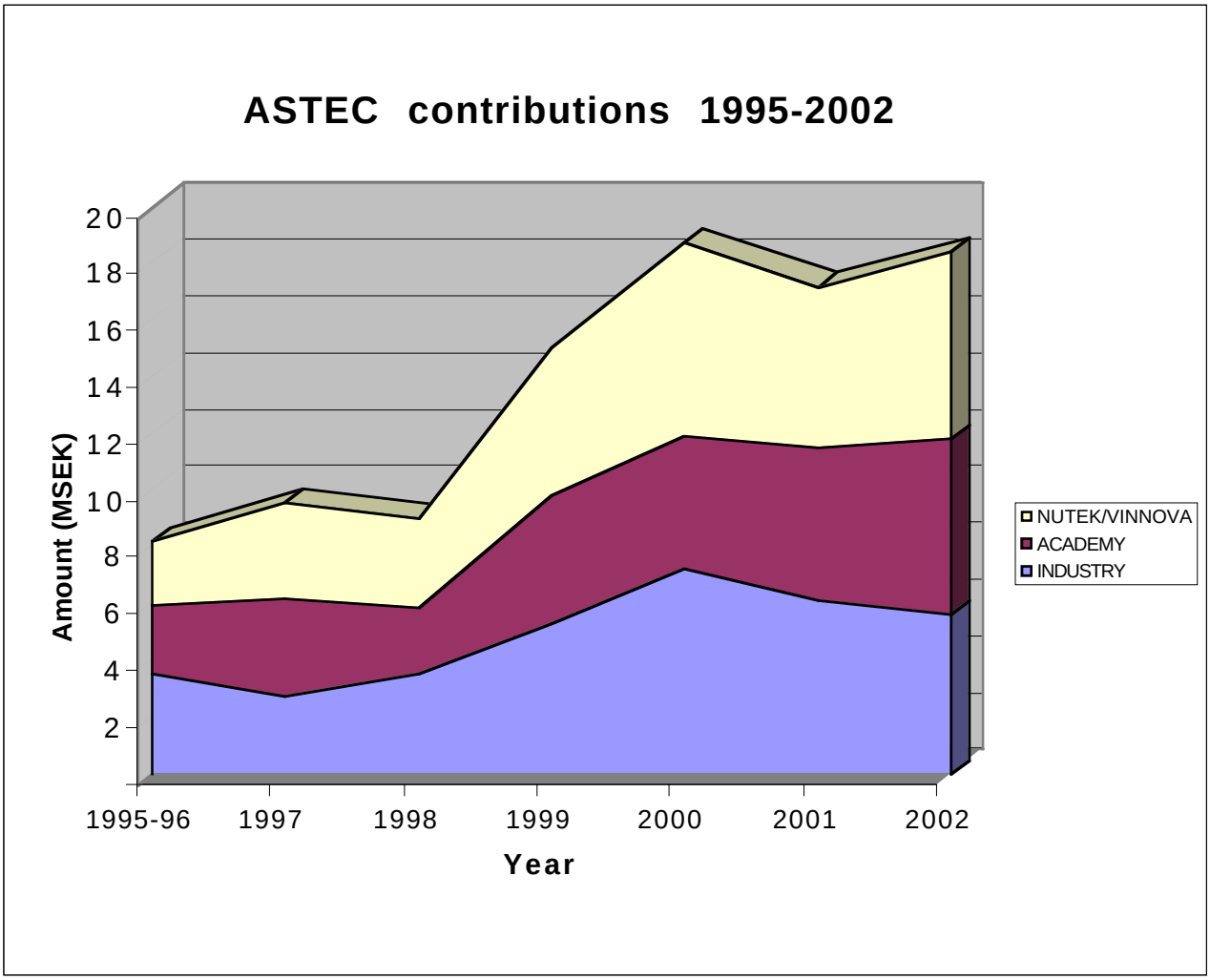
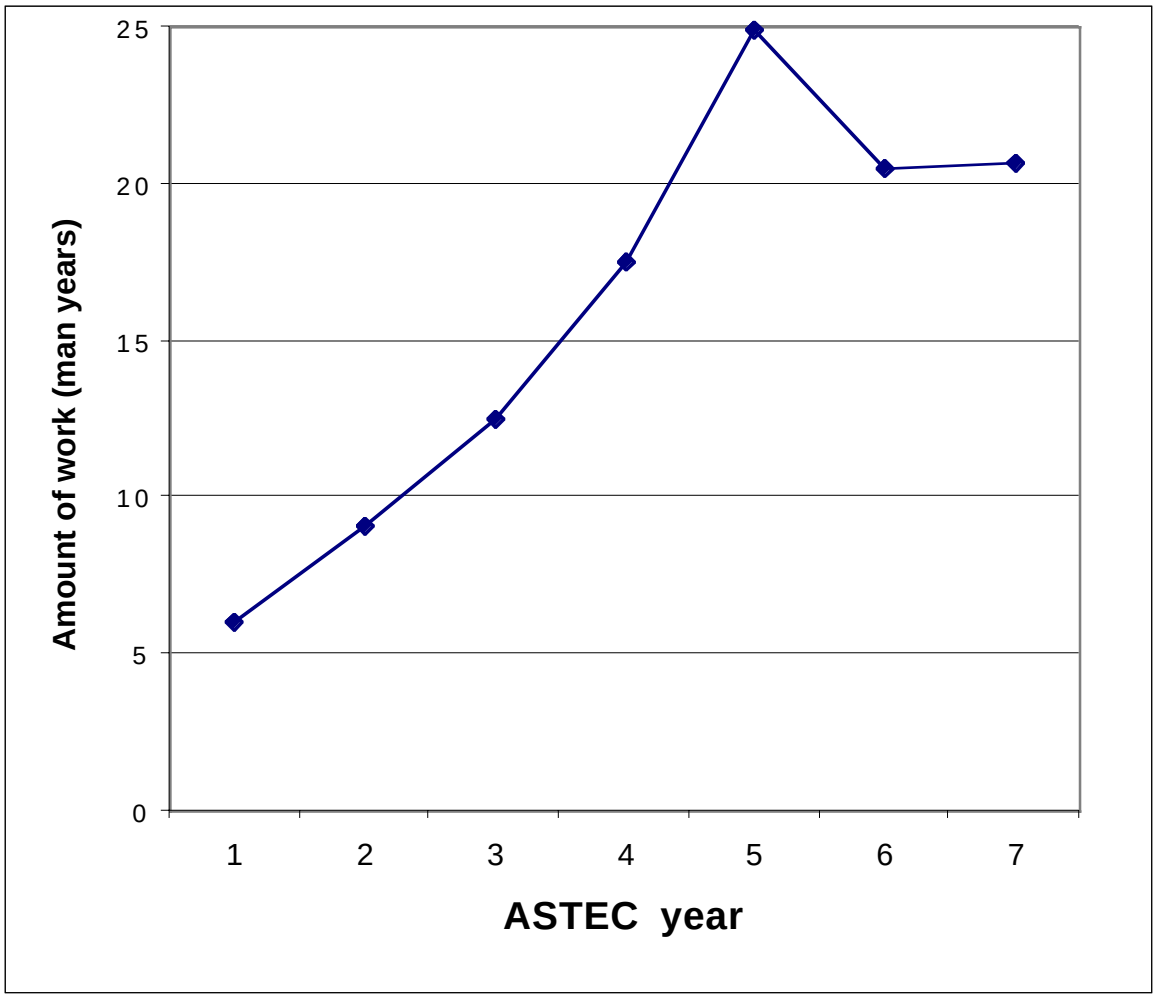
1b) The development of contributions to ASTEC by NUTEK, Academia and Industry.



2a) Development of work carried out within ASTEC in man years for each year.

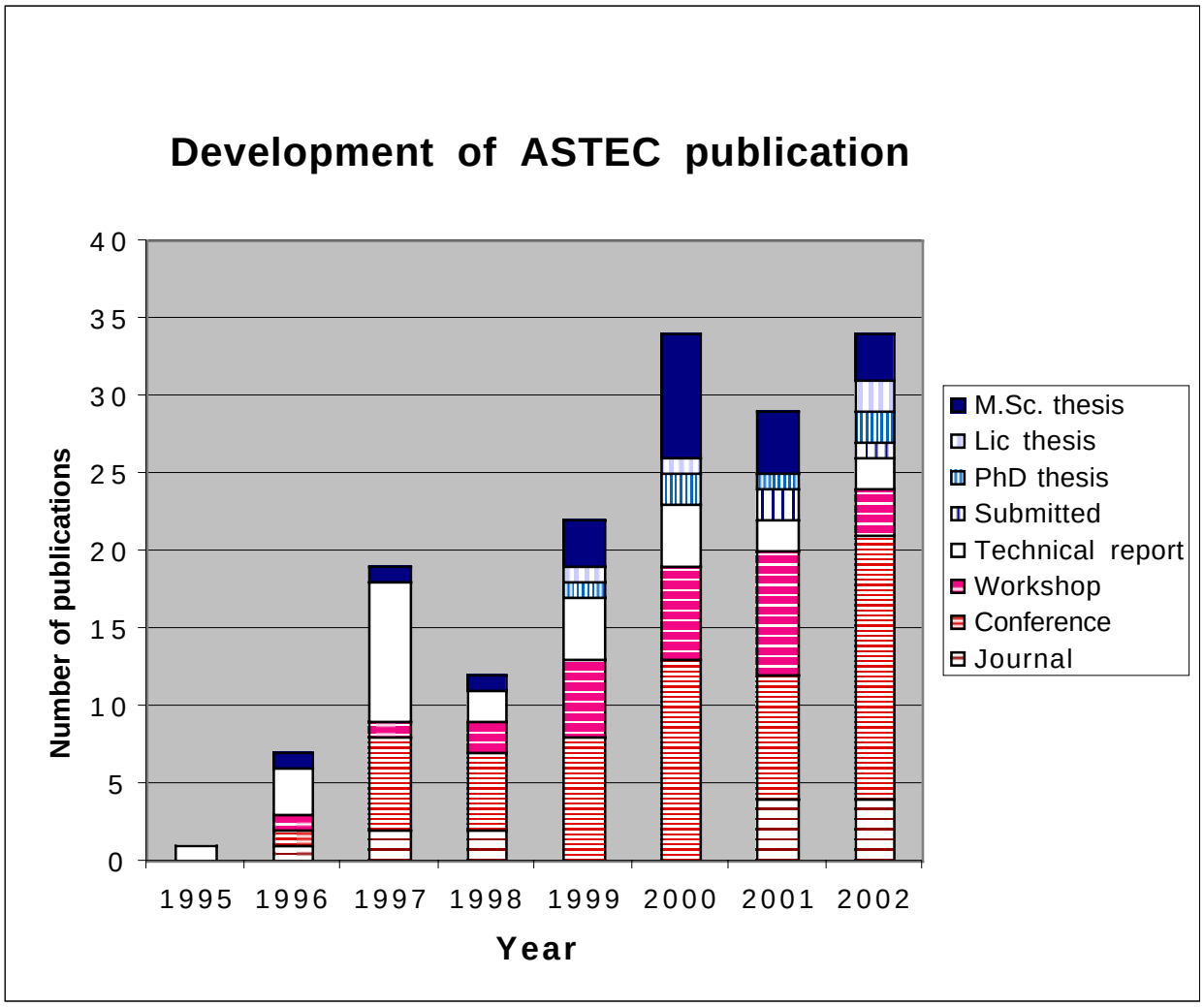


2b) Development of ASTEC staff categories,.

	Amount each year (man years)						
Category	**1995-1996**	**1997**	**1998**	**1999**	**2000**	**2001**	**2002**
Professor	0,5	0,3	0,6	0,6	2,1	1,8	1,4
Senior researcher	1,2	2,1	2,5	4,1	2,8	2,4	2,1
PhD student	3,3	4,1	6,3	7,1	9,0	7,1	10,6
Industry researcher	1,0	1,7	2,2	2,1	3,8	1,7	2,5
Industry PhD students				2,0	3,0	4,0	1,9
Master of Science students				1,0	3,9	3,2	1,9
Technical/administrative		1,1	1,0	0,6	0,5	0,4	0,3
Total=	6,0	9,1	12,5	17,5	25,0	20,5	20,7
Increase each year (man years)	-	3,1	3,4	5,0	7,4	-4,4	0,2
Increase each year (%)	-	52%	37%	40%	42%	-18%	1%

Publications and exams

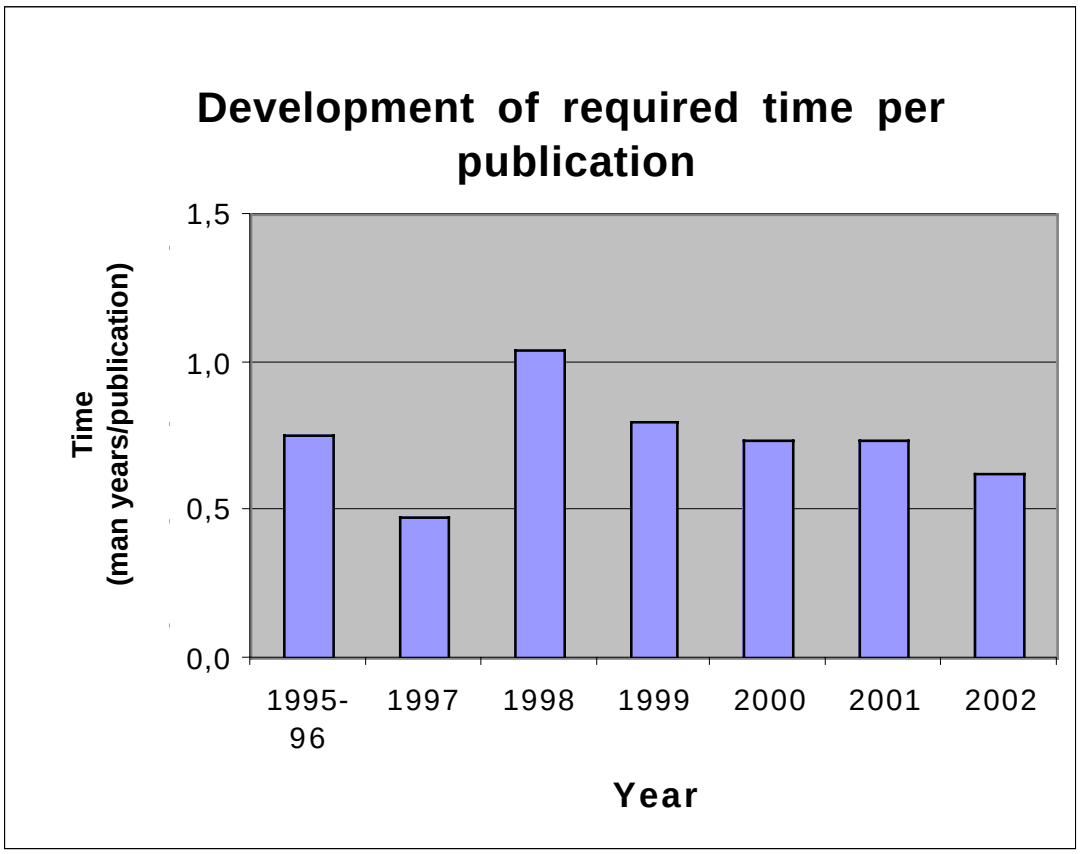
3a) Publication rate, note the increase following each phase initiation in 1995, 1998 and 2001.



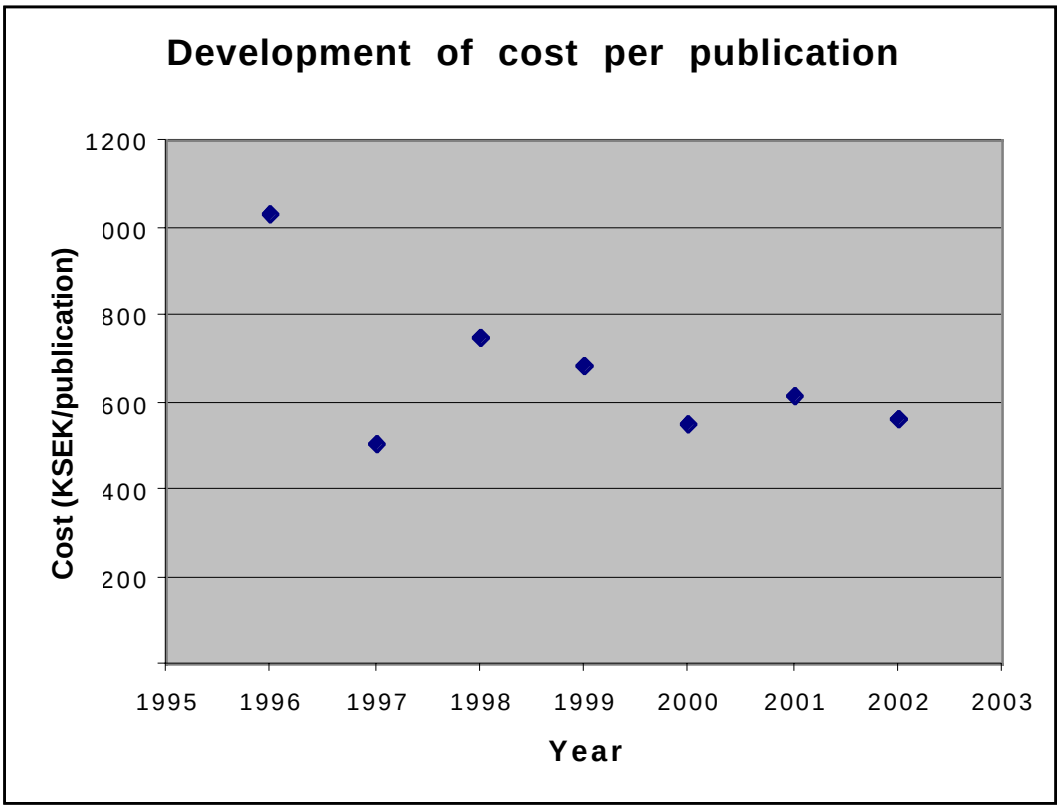
3b) Publication divided into different publication categories, note the increase in journal publication and that conference, workshop and technical reports are dominating.

Publications type	year								
	1995	1996	1997	1998	1999	2000	2001	2002	Sum
Journal		1	2	2			4	4	13
Conference		1	6	5	8	13	8	17	58
Workshop		1	1	2	5	6	8	3	26
Technical report	1	3	9	2	4	4	2	2	27
Submitted							2	1	3
PhD thesis					1	2	1	2	6
Lic thesis					1	1		2	4
M.Sc. thesis		1	1	1	3	8	4	3	21
Sum	1	7	19	12	22	34	29	34	158

3c) Time requirement and cost per ASTEC publication, note the decrease in time per publication as a new phase develops. Phase 1 started 1995, phase 2 started 1998 and phase 3 2001.



3c) The cost per ASTEC publication, note the trend in decreasing cost per publication over time.



Financial report for ASTEC year 2001 and 2002 and budget for2003

Uppdated 2003-06-05

			Beräknat	see note **	Phase 3		
	Budget 2001	**Result 2001**	**Resultat 2002**	**Budget 2003**	kr	division	Comments
ABB Automation Products	112 000	103 000	-	490 000	593 000		2003 only ABB robotics
Cross Country Systems AB	500 000	150 000	150 000	-	300 000		
ENEA OSE Systems AB	280 000	287 230	261 000	261 000	809 230		58 kUSD donation
Ericsson Utvecklings AB	2 550 000	2 326 080	1 581 680	560 000	4 467 760		
ESAB	25 000	-	-	-	-		
I.A.R. Systems AB	2 500 000	2 371 200	1 696 020	1 000 000	5 067 220		
Prover Technology AB	800 000	200 000	1 800 000	325 000	2 325 000		Uncertain if the 2002 funds can be counted.
Telelogic Sverige AB	500 000	200 000	-	-	200 000		
Validation AB	675 000	382 500	119 000	675 000	1 176 500		
Virtutech AB	300 000	-	51 200	448 000	499 200		
Volcano Communicaton Technologies AB	150 000	-	-	100 000	100 000		
Volvo Teknisk Utveckling AB	150 000	97 000	-	150 000	247 000		
Mobile Arts	-	-	-	800 000	800 000		Suggested as new partner from 2003-01-01.
T-mobile				449 940	449 940		Suggested as new partner from 2003-01-01.
New partner or increased contributions				965 150	**965 150**		
Industry	8 542 000	6 117 010	5 658 900	6 224 090	18 000 000	34%	
Uppsala Universitet inkl MDH	4 262 407	4 125 542		4 473 046			
SICS	1 060 800	307 413		-			
MDH		959 030		959 030			
Akademy	5 323 207	5 391 985		5 432 076	16 256 138	31%	
VINNOVA**	6 000 000	5 711 969		6 303 501	18 000 000	34%	
SUM	19 865 207	17 220 964		17 959 667	52 256 138	100%	

* Original budget the same contribution each year, the amounts are given in the column "Budget 2001".

** ASTEC managemet budget assumption of contributions for 2003.

*** VINNOVA funding amounts is shown as the year they are consumed. The payment of the contribution is exactly 6 MSEK per year.

ASTEC Cash report

Appendix 5

Cash flow

	Result 2001	Result 2002	Budget 2003	Comments
Income	**kr**			
Contribution from VINNOVA/NUTEK	3 000 000	7 500 000	4 500 000	
Advance payment	3 717 096	2 335 013	2 870 483	
From Ericsson to HiPE project	700 000	600 000	220 000	
From T-Mobile to HiPE			449 940	
From ESAB to CODER	-			
Interest+ pension refunding	108 340	119 292	100 000	
Sum	**7 525 436**	**10 554 306**	**8 140 423**	
Advance payment within projects				
HIPE	378 583	573 000		
SA	527 824	-		
Sum	**906 407**	**573 000**	**-**	
Projects				
CODER	-	-	-	
TAS	-	-	-	
WCET in Uppsala	855 291	660 712	117 221	3 months 2003
WCET in Västerås (delayed payment 01)	-	1 126 650	395 720	
WPO	758 505	463 245	359 764	
HiPE	1 561 000	*2 657 031*	735 365	exkl T-mobile
ErlVer	307 413	-	-	
SA	134 266	-	-	
SAAPP	-	419 616	468 883	
Automated testing	141 667	468 650	468 883	
SMC (delayed payment for 2000 & 2001)	200 000	813 825	234 441	
Software Synthesis	655 000	705 550	468 883	
Analysing ERLANG/OTP systems	212 500	380 242	-	
STEP			234 441	Mobile Arts project
REMODEL			245 000	ABB robotics project
Summa projekt	**4 825 642**	**7 695 521**	**3 728 599**	
Administration, kick-off, pr, etc				
Tax (Högskolemoms 8% on Ericsson to HiPE)	56000	0	35 995	
Administration, Kick-off etc	606 327	556 927	739 375	2003 inkl. ass. manager
Tillfällig justering		- 4 375		
Equipment	35 861			
Calculated advance payment 2003-12-31	2 335 013	2 870 483	**3 636 454**	
			Left for disposal during phase 3	
		Amount possible to use ===>	**2 671 304**	

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