ASTEC Advanced Software Technology

Report for year 3, 1998

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Introduction

The enclosed document is the report from the competence center Advanced Software Technology (ASTEC), for the period 1998-01-01 - 1998-12-31. The structure of the document follows closely the guidelines given by NUTEK. The document summarizes the activities in ASTEC during year 3. Other up-to-date information about current activities can be found on the WWW page http://www.docs.uu.se/astec/ Uppsala, May 1998

Professor Bengt Jonsson, director

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Summary

ASTEC (Advanced Software Technology) is a competence center which focuses on Advanced Tools and Techniques for Software Development. Development of software accounts for a significant part of the costs in the construction of major products, such as communication and process control systems, of Swedish industry. An important means to produce better software at lower cost is to employ software technology in the form of high-level specification and programming languages, supported by powerful automated tools that assist in specification, analysis, validation, simulation, and compilation. The purpose of ASTEC is to conduct research on pre-competitive industrially applicable techniques for software specification, design, and implementation at a high level of abstraction, and to be a forum for contacts and exchange of ideas between academia and industry.

The year 1998 has been a "restructuring" period for ASTEC, during which the research activities have been guided by a strategic research plan. The main ideas behind the strategic plan were to promote longer-term research projects, suitable for Ph.D. thesis work within an area where the partners of ASTEC have strong competence, and with a potential for expansion of industrially relevant research activities. In addition, fora for collaboration and exchange of ideas between projects have been organized.

During 1998, the new strategic plan has proven to be a viable foundation for ASTEC work. Evidence of this is that the industrial involvement is increasing, that new projects fall naturally into the lines of the strategic plan, and that a number of Ph.D. theses are well in progress.

Sammanfattning

ASTEC (Advanced Software Technology) är ett kompetenscentrum som sysslar med avancerade verktyg och tekniker för programvaruutveckling. Programvaruutveckling står för en betydande del av kostnaderna vid konstruktion av många viktiga produkter inom svensk industri till exempel kommunikationssystem och processtyrsystem. Ett viktigt led i att kunna producera programvara av högre kvalite till lägre kostnad är att använda språk för att specifiera och programmera på en hög abstraktionsnivå, som stöds av verktyg för specifiering, analys, validering, simulering och kompilering. ASTECs syfte är att bedriva forskning kring industriellt användbara tekniker för programvaruspecifiering, -konstruktion och -implementering på en hög abstraktionsnivå, och att utgöra ett forum för kontakter och ideutbyte mellan akademi och industri.

För ASTEC har1998 varit ett år av "omstrukturering". Forskningsplaneringen har styrts av den strategiska plan, som utarbetades under hösten 1997. De bärande ideerna bakom den strategiska planen har varit att befordra långsiktiga forskningsprojekt som lämpar sig för avhandlingsarbete inom ett område där ASTECs parter har stark kompetens och där det finns potential för att expandera industrirelevant forskning. Dessutom har ett antal former för samarbete och informationsutbyte organiserats.

Som slutsats av 1998 kan man säga att den strategiska planen visat sig vara en god grund för fortsatt utveckling inom ASTEC. Tecken på detta är att det industriella engagemanget ökar, att nya projekt på ett naturligt sätt kan definieras i enlighet med planen, och att ett antal doktorsavhandlingar är på gång.

Development of Research Activities

The year 1998 has been a "restructuring" period for ASTEC, during which the research activities have been guided by the strategic research plan , developed at the end of 1997. The main ideas behind the strategic plan were to:

- Focus research planning and activites to a suitaby focussed area, in which the partners of ASTEC have strong competence, and with a potential for expansion of industrially relevant research activities.
- Put the main emphasis of research on PhD work. This means that most projects must be sufficiently long-term to form the basis for Ph.D. work.
- Create organized fora for collaboration and exchange of ideas between projects. These fora include regular seminar series in the program areas, a series of ASTEC seminars, and discussions at companies.

The strategic research plan has proven to be a viable foundation for the activities in ASTEC. This is supported by the following general observations at the end of 1998.

- The companies that have been part of the ASTEC consortium in 1998 will continue, and in several cases expand, their involvement during 1999-2000. There is one exception (Rational Software Scandinavia), which leaves ASTEC mainly beyond the influence of ASTEC.
- 5 new companies will join ASTEC in 1999. One of these (UPAAL AB) is formed as a result of ASTEC activities, to undertake tasks that can be conducted on a purely commercial basis.
- In planning for 1999, it has been found that the new projects follow the strategic research plan in a natural way.
- Most of the research in ASTEC is part of Ph.D. thesis work. At the end of 1998, ASTEC supports 10 Ph.D. students, 2 of which are industrial Ph.D. students. 4 Ph.D. theses are expected in 1999 as a result of ASTEC work.
- During 1998, 8 projects have been conducted, 5 of these will continue within ASTEC in 1999, and one project will continue to completion outside ASTEC. Of the terminated project one will be followed by a continuation project in 1999, and the other project died prematurely.

The research activities of ASTEC are structured into program areas. A program area is identified with a line of research for solving specific problems combining clear industrial relevance with research challenges. It focuses the efforts from several projects and is responsible for a wider dissemination of the conclusions, conducting seminars or specialised courses as deemed necessary. The areas are interrelated in that progress in one area is dependent on the state of the art in the others for

maximal impact.

After the development of the Strategic Plan during late 1997, ASTEC runs research structured into three technical program areas, which serve to develop techniques for software development, and two areas, where techniques are applied and evaluated for specific types of software systems. A particular project can very well span over several of these areas. Most projects will span over at least one technical area and one application area.

The technical areas are

1. Validation and Verification Technology , concerned with high-level notations for expressing requirements and design specifications, as wel as tools for analysis for verification, validation, test generation, and tracing of requirements.
2. Programming Languages and Implementation Technology , concerned with design, use, and implementation of very high-level programming languages, as well ass efficient compilation for different target architectures.
3. Technology for Real-Time Distributed Systems , concerned with features specific to software development for embedded real-time and distributed systems, such as timing behaviour, distribution and failure handling.

The application areas are

1. Software for Automotive and Vehicle Applications There is a demand for an increasing number of functions in modern vehicles. Existing mechanical solutions are re implemented in software and new functions are added, which are impossible to implement without software solutions (for example see Volvo Tech Rep 1998 no. 1 pp 2-19 (http://www.tech2.volvo.se/reportage/main.htm). These functions may be safety-critical and/or equipped with important constraints on resource utilisation. This calls for highly predictable and fault tolerant software/hardware systems. Typically, software is deployed in the nodes of a distributed network with requirement for real-time behaviour.
2. Software for Data- and Telecommunication Systems Telecom software systems are often very large and there is a great interest in processes and methods. The area is undergoing drastic changes, recently there was mostly audial telephony: now mobility, interactive multimedia and the Internet are more important. Some characteristics of this area are high requirements on reliability, massive concurrency, high distribution, heterogeneity, stringent time-to-market requirements, ability to update systems with new functionality while in operation etc.

Thus, projects within ASTEC can be classified using a 2*3 matrix (Table 1).

Table 1. ASTEC projects per research area 1998

ASTEC Projects per Research Area	Validation and Verification Technology	Programming Languages and Implementation Technology	Technology for Real-Time Distributed Systems
Datacom and Telecom Applications	EriVer BOOM ARENA	HIPE	
Automotive and Vehicle Applications	Auto BOOM Vasaco	WCET WPD	Auto WCET

Some of the main trends in the research work of ASTEC, with respect to the strategic plan, have been:

- ASTEC has become committed to the build-up and consolidation of strong research in the three technical program areas Validation and Verification , Programming Languages and Implementation , and Real-Time Distributed Systems . Several new recruited faculty members at the concerned departments are experts in these areas.
- In comparison with phase 1, the work on programming language implementation, including optimizing compilation, has reached a large volume, and has obtained industrially significant results. Links with other areas (e.g., execution time analysis) are being established.

- The longer-term projects have developed some quite significant systems (Erlang Verification System, UPPAAL, HIPE compiler), which require a significant amount of manpower, but allow to conduct larger case studies that can say something about industrial applications.
- The initial work on requirements, focussing on UML and on requirements handling, is approaching its completion. A thesis on UML is expected during 1999.

The development of research activities per program area.

Validation and Verification Technology

The area considers methods and tools for analysing the correctness of systems and system components. Emphasis is on formal approaches to requirement and design specification, and on methods and tools for establishing adherence of systems to their specifications. The major foci of work are the following

- Formalisms One of the major goals of ASTEC in this area is to develop a formal semantics for the newly appeared formal notation UML (Unified Modeling Language). ASTEC has participated in the development of UML. Within the project BOOM, the major goal is to develop a meta-language, named ODAL, in which the semantics of object-oriented specification notations can be given. During 1998, this work has progressed, almost to completion. A formal semantics of ODAL has been produced, forming the backbone of the forthcoming PhD thesis by Gunnar Övergaard.
- Analysis tools A first public release of a powerful analysis tool the "Erlang Verification Tool" has been produced. A first significant case study started during the latter part of 1998. A first report on this case study (a part of the Mnesia database system in the Erlang-based Open Telecom Platform will be finished by early 1999).
- Requirements The work on requirement handling has been concluded. Important aspects of a methodology for requirements handling and tracing were developed. Further developing this methodology, and extending it to further stages of the software engineering process requires new partners to enter the activity, with competence in tool development and test generation. A second source of requirements specifications could be useful. These efforts have resulted in a completely redefined project, with a focus on testing.

For the next period, several new projects are being planned in this area:

- Symbolic Model Checking will develop and evaluate new techniques for automated verification of programs and hardware circuits. The techniques are based on Stålmarck's algorithm for proving formulas in propositional logic, and could be much more powerful than existing methods.
- AF100 is a case study, involving ABB Automation and the new company UPAAL, where formal modeling and model-checking technology will be applied to gain increased understanding of and confidence in a bus protocol currently employed for communication in industrial control systems.
- Automated Testing will develop and evaluate techniques for increasing the degree of automation in current techniques for testing software and embedded systems. In particular, different techniques for automatic and semi-automatic generation of test sequences will be considered.

Programming Languages and Implementation Technology

The area considers finding and defining useful abstractions, i.e. programming language features that hide the details of low-level mechanisms, and their efficient implementation. Most of the work in the area has concentrated on efficient implementation of abstractions, in particular on developing techniques for producing more efficient code, and on evaluating these on programs taken from industrial practice. Two lines of research are pursued.

- Programs for Data- and Telecommunication Systems The main efforts here have concentrated around the HIPE compiler, an optimizing compiler for the Erlang programming language. The main contributions is that one is able to study the effect of optimizations on a real industrial programming language. The main effort during 1998 was the engineering of HIPE from its initial design to a stable, working system. This was completed in September, at which time benchmarking of a real-world telecom application (AXD301/scct) began. Measurements using this application are still going on. They have uncovered a variety of bottlenecks in the current Erlang implementation, for which improvements will be suggested and implemented in 1999.
- Programs for small Embedded Processors The main efforts here have been to implement and evaluate a collection of whole-program analyses and optimizations: a static profiler, an

alias analyzer, a memory allocator for irregular memories, and a technique for removing the C runtime stack for a class of programs. These optimizations have been performed inside the C-compiler of IAR Systems AB, which makes it possible to evaluate their effect on programs in actual use.

For the next period, a new project is being planned in this area:

- Static Analysis will develop techniques for analyzing run-time properties of Erlang programs from their code. The analyzed properties will be of used both for debuggging, for verification, and for compilation.

Technology for Real-Time Distributed Systems

The area considers techniques that are particular for building distributed embedded systems. Two main lines of research are pursued:

- Execution Time Analysis The goal of the project is to develop execution time analysis to the point where it can be incorporated into commercial tools. During 1998, the work on automatically annotating programs with bounds on the number of iterations of loops, and other similar bounds, has progressed so that a thesis is expected in 1999. Work is in progress for investigating how to build a commercial tool; investigations have been performed regarding the structural properties of existing code in industrial embedded applications.
- Development Methods for real-time distributed systems have been considered. The work pursued during Phase 1, using the UPPAAL tool for modeling and analyzing automotive applications, has been concluded. During the year, a new line of work, focussing more on the design notations actually used by Mecel AB, such as Software Circuits, has started.

The development of research activities per application area.

The research work in the Application areas overlaps with work work in the technical areas. Therefore, we report only on the aspects which are most directly relevant to respective applications.

Automotive Applications

- The work pursued during Phase 1, using the UPPAAL tool for modeling and analyzing automotive applications, including a gearbox controller, has been concluded. Part of the work is reported in an invited contribution to the journal Software Tools for Technology Transfer .
- A seminar on software technology for Automotive Applications was conducted in April 1998, with around 90 participants.

Datacom and Telecom Applications

- Work has been conducted on major case studies, taken from existing systems implemented in Erlang: a part of the Mnesia database system in the Erlang-based Open Telecom Platform, and the code in the AXD301/scct switching system.

Progress Reports from Different Projects

ErlVer

The most significant task in the ErlVer project for 1998 has been the public release of a prototype Erlang Verification Tool. This tool is to serve as the means for a practical evaluation of the utility of a novel approach to verification of distributed systems. The implementation of the tool required some foundational work, such as the development of a formal operational semantics for the core fragment of Erlang we focus on, and the development of a property specification language tailored towards Erlang programs. The approach and the results obtained were made known through several publications: one invited paper, two conference papers and two workshop presentations. A major case study was begun addressing a real-life application developed at Ericsson's Computer Science Lab.

BOOM

The BOOM project will develop the formal syntax and semantics of a meta-language for formal specification of modelling concepts. The language should be developed so it can be used for specifying several different modelling languages. Furthermore, the project will apply this language to the Unified Modeling Language, resulting in formal specifications of the different object concepts, relationships (like generalization, association, and aggregation), communication semantics, parallelism etc. The major impact from the project will be a formal object-oriented language to be used for specification of general object-oriented modelling

concepts, together with the formal specification the Unified Modeling Language. The results will, in general, facilitate comparisons between different methods and between different models. In a broader sence will the companies using formally specified modelling languages gain better understandings and interpretations of the systems they are developing. The project also contributes to the development of an industrial standard of object-oriented modelling languages.

ARENA

The investigation how the methodology can be further developed, and how it can support further stages of the software engineering process should be continued. This requires that new partners enter the project, with competence in tool development and test generation. A second source of requirements specifications could be useful. These efforts have resulted in a completely redefined project, with a focus on testing. This was partly a result of a reorganisation at Telia, where the Requirements Lab was discontinued. Telia Validation is one of the partners in the new project.

VASSCO

In this project, UU was supposed to assist Prover in the Esprit project CRISYS: Critical Instrumentation and Control Systems, and to dig deeper scientifically in areas covered shallowly by the project. The time until the start of CRISYS (January 1998) was used for scientific preparation. Around April 1998, it became clear that Prover was unable to or uninterested in providing CRISYS documents to UU. We received one document related to CRISYS by another channel. In May 1998, the PhD student quit and the project died silently.

HIPE

The main effort during 1998 was the engineering of HIPE from its initial design to a stable, working system. This was completed in September, at which time benchmarking of a real-world telecom application (AXD301/scct) began. To support accurate cost analysis, HIPE was extended to perform low-level profiling using the UltraSPARC's "performance counters". Using this facility, it is possible to count machine cycles spent in user code, the runtime system, and the OS kernel, as well as cycles spent waiting for cache misses in the three areas. This is an important tool when investigating system-wide behaviour and the effects of compiler or runtime system changes.

Towards the end of 1998, a small informal group was formed with the purpose of designing a new intermediate representation for Erlang, Core Erlang. Core Erlang will provide a common high-level interface between Erlang frontends, intermediate-level analysis and optimisation tools, and Erlang backends. The group currently consists of Robert Virding from Ericsson CSLAB, Richard Carlsson and Sven-Olof Nystrm from UU, and the members of the HIPE project.

WCET

The first steps of implementing a WCET tool and integrating it with a compiler from IAR systems has been taken. A paper describing our platform constructing this WCET tool has been submitted to a Real-Time Journal. The work on the tool will continue during the 1999 by implementing features needed for doing cache and pipeline analysis. Plans are present for at least two more articles. One PhD thesis concentrating on high-level flow analysis is planned to be completed during autumn 1999.

Our work on investigating real embedded system programs has resulted in two published papers. We have compared embedded programs and the common SpecInt95 benchmarks, and concluded that there is a clear need for benchmarks specific for embedded systems. The investigation has also given us valuable input for our WCET tool construction plans.

- The first steps of implementing a WCET tool has been taken. The tool will be integrating WCET analysis into a compiler from IARs system. The outline of the tool is described in [Ref3]. The work on the tool will continue during 1999, by implementing a hardware simulator which will be needed for doing pipeline analysis. A paper describing how to model pipeline effects in the execution time is planned to be submitted to the RTCSA'99 (Real-Time Computing Systems and Applications) workshop in Hong Kong. Other papers describing other parts of WCET analysis is also planned.
- The cooperation with IAR systems is running smoothly since Jakob, as an industrial PhD student, communicates with people from IAR and from Uppsala University.
- The network of WCET researchers within Sweden are continuing with their cooperation. The last meeting where in Västerås during April where WCET researchers from Västerås, Lund and Uppsala met.

Financial report

The contributions by each ASTEC partner during 1998 is summarized in Table 2. The actual contributions exeeded the planned contribution with 5.6% (515 kkr). This was achived by an 18% increase in the companies contributions. During 1998 were the main efforts were put on the areas "Validation and Verification Technology" and "Programming Languages and Implementation Technology" with an even distribution per application area (Tables 1 and 3).

A part of Ericsson´s contribution were recived as cash (Table 2) all other contributions represents work carried out by the companies. These contributions has been reported either as time used by employees which thereafter has been transferred to SEK by multiplication with a standard factor of 900 kkr per man year or by directly reporting a sum in SEK based on the companies internal prices.

Table 2. Financial report for ASTEC 1998

Year 3 compared to contract.		Contract		Result 1998		Comparision Change	
		kkr	%	kkr	%	kkr	%
Industrial partners		3330	36,4	3929	40,7	599	18,0
Uppsala Universitet inkl SICS och KTH		2960	32,4	2876	29,8	-84	-2,8
NUTEK		2850	31,2	2850	29,5		0,0
	Total=	9140	100	9655	100	515	5,6
Contribution by companies during 1998							
Ericson Telecom AB (940 kkr was cash contrib)		1240		1390		150	12,1
IAR systems AB		1200		1493		293	24,4
Mecel AB		360		249		-111	-30,8
NP Technology AB (Prover AB)		180		385		205	113,9
Rational Software Scandinavia AB		150		256		106	70,3
Telia Validation AB		200		156		-44	-22,0
	Total=	3330		3929		599	18
Contribution by academy and research institutes							
SICS				1080			
Uppsala University +KTH				1532			
Management and administration at UU				264			
	Total=			2876			

Table 3. ASTEC contributions per research area 1998

ASTEC Results 98 **per Research Area** **(% of total)** Administration not included.	Validation and Verification Technology	Programming Languages and Implementation Technology	Technology for Real-Time Distributed Systems	Sum
Datacom and Telecom Applications	26,7	16,8	0,0	43,5
Automotive and Vehicle Applications	20,2	24,6	11,7	56,5
Sum	46,9	41,4	11,7	100,0

Staff during 1998

The staff has increased during 1998. There are 3 new PhD students, 2 new senoir scentists and 4 new industrial staff persons engaged in ASTEC. Four persons that were active in phase 1 has turned to other tasks.

Academic staff

Name	Affiliation	Category	Amount	Projects
Tobias Amnell	UU	Ph.D. student	0%	Auto
Dirk Auchter	UU	Ph.D. student	80%	VassCo
Roland Bol	UU	Senior	35%	ARENA/VassCo
Gennady Chugnov	SICS	Ph.D. student	40%	ErlVer
Mads Dam	SICS	Senior	20%	ErlVer
Jakob Engblom	UU/IAR	Ph.D. student	40%	WCET
Andreas Ermedahl	UU	Ph.D. student	80%	WCET
Lars-Åke Fredlund	SICS	Ph.D. student	80%	ErlVer
Bo Frödeberg	UU	Ph.D. student	60%	WPO
Dilian Gurov	SICS	Post Doc	80%	ErlVer
Roland Grönroos	UU	Admin	8%	Management
Hans Hansson	UU	Senior	10%	WCET/AUTO
Erik Johansson	UU	Ph.D. student	80%	HIPE
Christer Jonsson	UU	Res. Eng.	75%	HIPE
Bengt Jonsson	UU	Prof.	42%	Management
Thomas Lindgren	UU	Senior	20%	WPO/HIPE
Sven-Olof Nyström	UU	Senior	20%	WPO
Helena Petterson	UU	Admin	10%	Management
Joachim Parrow	KTH/UU	Prof.	19%	BOOM
Mikael Pettersson	UU	Senior	58%	HIPE
Paul Pettersson	UU	Ph.D.student	30%	AUTO
Wang Yi	UU	Senior	10%	AUTO
Gunnar Övergaard	KTH	Ph.D. student	60%	BOOM

Industrial staff

Name	Company	Amount
Thomas Aarts	ETX	50%
Parosh Abdulla	Prover Technology	30%
Anders Berg	IAR	20%
Arne Borälv	Prover Technology	2%
Jan-Erik Dahlin	IAR	10%
Bjarne Däcker	ETX	Board
Jakob Engblom	UU/IAR	35%
Mats Fors	IAR	5%
Tomas Grelsson	Telia	2%
Sten Hellström	Mecel	Board
Olle Landström	IAR	Board
Magnus Lindahl	Mecel	28%
Stefan Mangenat	Telia	16%
Karin Palmqvist	Rational	1%
Anders Pikas	IAR	5%
Carl von Platen	IAR	5%
Åke Sandberg	Telia	Board
Jan Sjödin	IAR	5%
Mikael Strömberg	Mecel	1%
Håkan Törngren	IAR	5%

Contracts

All contracts within ASTEC are listed in table 4. No new contracts were made as a result of year 3. Most contracts are written in Swedish therefore is this text partly in Swedish.

Table 4. All contracts within ASTEC

Avtals namn	Avtalet avser	datum	Upphör	Parter
Avtal	överlåtelse av resultaträttigheter	1995	Hängavtal etapp 1	UU, Björn Carlsson
Avtal	överlåtelse av resultaträttigheter	1995	Hängavtal etapp 1	UU, Mats Carlsson
Avtal	överlåtelse av resultaträttigheter	1995	Hängavtal etapp 1	UU, Roland Bol
Avtal	UU-KTH-SICS samarbete	95-10-17	97-08-31	UU, KTH, SICS
Avtal	överlåtelse av resultaträttigheter	95-10-24	Hängavtal etapp 1	UU, Johan Blom
Avtal	överlåtelse av resultaträttigheter	95-11-23	Hängavtal etapp 1	UU, Hans Hansson
Project background	Ericson Engineering Tool	95-12-08		This is a claim by Ericsson
Avtal	överlåtelse av resultaträttigheter	1996	Hängavtal etapp 1	UU, Wang Yi
Avtal	överlåtelse av resultaträttigheter	1996	Hängavtal etapp 1	UU, Bengt Jonsson
Avtal	överlåtelse av resultaträttigheter	1996	Hängavtal etapp 1	UU, Andreas Ermedahl
Avtal för NUTEK kompetenscentrum ASTEC etapp 1	ASTEC etapp 1	96-01-11	97-08-31	UU, NUTEK, Ericsson, IAR, Logikkonsult, Mecel, Objektory, Telia.
Sekretessavtal för kravspec 1095-FSA AXAA101		96-01-15	vid projektslut	Telia, UU.
Bakgrundsrättigheter	NP-Tools 2.1	96-06-12		UU, Telia, Mecel, Objectory, Logikkonsult, Ericsson, IAR, SICS.
Avtal	överlåtelse av resultaträttigheter	96-11-27	Hängavtal etapp 1	UU, Jens Larsson
Avtal	överlåtelse av resultaträttigheter	96-12-06	Hängavtal etapp 1	UU, Hans Börjesson
Avtal	överlåtelse av resultaträttigheter	96-12-10	Hängavtal etapp 1	UU, Jan Gustavsson
Project background	UPPAAL	97-02-17		This is a claim by Wang Yi
Avtal för NUTEK kompetenscentrum ASTEC år 3	ASTEC år 3 saknar start datum efter 98-02-05		98-09-30	UU, NUTEK, Ericsson, IAR, Logikkonsult, Mecel, Objektory, Telia.
ABB subcontract agreement	AF100 protocol	99-04-14		ABB, UPAAL, UU
Avtal för NUTEK kompetenscentrum ASTEC etapp 2	ASTEC etapp 2	pågår		
Avtal	UU-SICS samarbete	inväntar ASTEC etapp 2 avtalet		UU, SICS
Avtal om immateriella rättigheter	förvärv och ersättning för rättigheter	inväntar ASTEC etapp 2 avtalet		UU, näringsliv
Avtal	överlåtelse av resultaträttigheter	inväntar avtal om immaterialrätt		UU, forskare

Effect on Environment

One of the goals of ASTEC is to develop techniques for reducing memory requirements by producing compact object code and allocating data efficiently. Using less memory in, e.g., a mobile phone, implies using fewer and simpler hardware components, which results in a lower burden on the environment during manufacture and disposal of the product. Using less memory will also reduce power consumption, which is particularly significant in portable systems powered by accumulators.

More indirectly, the validation techniques developed by ASTEC serve to make safety-critical software more reliable. Some safety-critical software, e.g., in nuclear reactors, is connected with environmental risks, and if applied to such systems, the techniques developed by ASTEC can reduce these risks.

Collaboration

As part of implementing the strategic plan, several forms of collaboration within ASTEC have been put forward. These include

- Regular workshops in Program areas. During 1998, one workshop on Verification tools was conducted in Linköping. One seminar on software for automotive systems was conducted in Gothenburgh.
- Discussions hosted by industrial companies, on aspects of software technology, have been conducted at most of the companies in ASTEC.
- A lot of efforts has been put on development of collaboration at the prospect of phase 2. The new collaboration plans have been included in the present version of the general plan.

Results and Effects

The major results for research

- The HIPE compiler has been completed into a working system. Early results indicate that HIPE achieves speedups ranging from a factor of two on the AXD301/sctt telecom application, to a factor of 17 on smaller programs. Measurements indicate that AXD301/scct spends more than half of its execution time in the Erlang runtime system or the OS kernel, and that further improvement of the efficiency of the Erlang system must consider the runtime system itself together with system-wide analysis and optimisations.
- A prototype Erlang Verification Tool has been publicly released. This tool is able to build proofs of properties of programs written in a subset of the Erlang programming language. A major case study -- a distributed database server -- is in progress.
- ASTEC has participated in the development of UML. ODAL, a meta-language for giving the semantics of object-oriented specification notations such as UML, has been completed.

The major results for industries

IAR Systems

We have during 1998 decided to add a second industrial theseis worker under the ASTEC program within IAR. This person (Jan Sjödin) will focus on optimizations in the compiler technology area within the WPO ASTEC project. This project is focusing on the very core technology area of IAR. The reason for this increased involvement in ASTEC is, of course, beacuse we are very happy with our first industrial thesis worker (Jakob Engblom) who has been active in the WCET project of ASTEC.

As of today, no new customer products have been developed but many new product ideas have been presented and a lot of knowledge has been transferred to IAR. This technology transfer includes direct research results as well as indirect knowledge about other interesting business areas and customer contacts.

Olle Landström .

Ericsson Utvecklings AB

Within the computer science lab, the ErlVer project resulted in a tool that is extensively used by Thomas Arts to verify part of the Mnesia code. The writer of the code, Hans Nilsson, became more interested in verification of software because of this project. This, on its turn, resulted in another verification attempt, viz. verification of the TCAP protocol.

Bjarne Däcker

Criteria for Evaluation

The criteria for a future evaluation of ASTEC should naturally follow the basic ideas and goals of ASTEC. These are to perform pre-competitive research on industrially applicable techniques within ASTECs scope, and to promote for contacts between research and industrial practice. Therefore, natural evaluation critera are a combination of

- scientific results and scientific impact, together with
- industrial results and industrial impact, and just as importantly
- how well ASTEC has managed to combine these two criteria.

It is also natural to evaluate the mutual impact on industry and academia of the work in ASTEC, in

terms of

- direct and indirect influence on industrial practice and products, and
- direct and indirect impact on the direction of academic research.

The internal evaluation of research within ASTEC is conducted in two ways:

- every 6 months, progress of projects is reviewed by the board, in terms of results and in terms of the collaboration between academia and industry.
- At sparser intervals, the research program and its development is reviewed by the scientific advisory board.

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